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*Semiconductor Measurement Technology:*

**Design and Testing  
Guides for the CMOS and  
Lateral Bipolar-on-SOI  
Test Library**

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J. C. Marshall and M. E. Zaghloul

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<sup>1</sup>At Boulder, CO 80303.

<sup>2</sup>Some elements at Boulder, CO 80303.

# *Semiconductor Measurement Technology:*

## **Design and Testing Guides for the CMOS and Lateral Bipolar-on-SOI Test Library**

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Abstract

Design and testing guides have been developed for the test library from which test chip NIST8 and test wafer NIST9 were derived. They were designed for use in process monitoring and device parameter extraction to evaluate and compare CMOS (Complementary Metal-Oxide-Semiconductor) test structures, including devices and circuits, fabricated on both bulk silicon and SOI (Silicon-on-Insulator), specifically SIMOX (Separation by the IMplantation of OXYgen), wafers. The test library consists of both CMOS-on-SOI and lateral bipolar-on-SOI modules. From it, 20 modules were assembled to create CMOS test chip NIST8 that was fabricated using a standard bulk CMOS foundry through the MO-SIS service. SOI/SIMOX test wafer NIST9 contains approximately 1000 modules and was also assembled from modules in this test library. Fourteen processing masks are used to fabricate depletion-mode MOSFETs, lateral bipolar devices, and CMOS MOSFETs with source-to-channel ties. The SOI/SIMOX technology file used with the Magic VLSI layout editor was modified to include the layers necessary to generate these 14 processing masks. This modification is discussed, and unique test structure designs are presented.

Key words: bipolar; CAD; CMOS; Magic; NIST8; NIST9; SOI; technology file; test chip; test structure

## 1. Introduction

This document is the design and testing guide for the generic test library from which test chip NIST8 and test wafer NIST9 were derived. This test library is intended for researchers in industry, university, and government laboratories who are initiating an SOI process. NIST8 and NIST9 were designed for process monitoring and device parameter extraction to evaluate and compare CMOS (Complementary Metal-Oxide-Semiconductor) test structures, including devices and circuits, fabricated on both bulk silicon and SOI (Silicon-on-Insulator) wafers. The test library was designed for the SOI technology known as SIMOX (Separation by the IMplantation of OXYgen).

From this library, a CMOS test chip NIST8 was assembled and submitted to MOSIS [1] for fabrication in a standard CMOS foundry on conventional bulk silicon wafers. Also, a lateral bipolar and CMOS-on-SOI test wafer NIST9 was assembled from this test library. An SOI/SIMOX process for the fabrication of NIST9 is described in section 2 to provide a brief process overview for sample test structure designs which will follow.

The SOI/SIMOX test chips NIST3 and NIST4 that preceded the design of the test library are described in the references [2,3]. A substantial number of additional designs are incorporated into the test library and are described in section 3. These designs include depletion-mode MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), lateral bipolar devices, and CMOS MOSFETs with source-to-channel ties that require 14 processing masks.

The "technology file" used with the CAD graphic layout editor Magic\*[4] was modified to include the layers necessary to realize the 14 processing masks needed to build the test library, as well as modifications made since NIST3 and NIST4 were built. This is discussed in section 4. Magic is running under OpenWindows 2.0 on a Sun SPARCsystem 300 running SunOS 4.1.2.

Section 5 describes the test library from which a variety of modules can be assembled to create a new test chip or test wafer, or the modules can be used as "drop-in's." This section explains the philosophy behind the module sizes, dimensions, placements, nomenclature, architecture, and so forth. Each one of the modules described in this section is designed to facilitate packaging.

NIST8 is a CMOS test chip that was assembled from 20 modules in the test library. It is

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\* In this report, commercial equipment, instruments, and computer programs are identified to specify the procedure adequately. This does not imply recommendation or endorsement by NIST, nor does it imply that the equipment or program is the best available for the purpose. In spite of the authors' experiences that the programs perform correctly on every set of data which has been tried, there can be no assurance that the program will perform equally well on all (possibly anomalous) data. Therefore, both the authors and NIST assume no liability for possible losses resulting from the use of these programs.

described in section 6 and is a CMOS-on-SOI design converted to a CMOS on bulk silicon design via the technology file. NIST8 was tested on the HP 4062UX Semiconductor Process Control System, and the testing results were evaluated using the computer procedure KEYS (linKing softwarE to analyZe waferS) [5]. KEYS links SUXES (Stanford University eXtractor of modEl parameterS) [6], SPICE (a Simulation Program with Integrated Circuit Emphasis) [7], and STAT2 [8] to facilitate integrated circuit evaluation. A simplified block diagram for KEYS is given in figure 1. The CMOS data from NIST8 can be presented and compared with the SOI/SIMOX data from NIST9 once it is fabricated and tested.

The SOI/SIMOX test wafer, NIST9, is presented in section 7. It describes its formation, organization, and the test structures that were included from the test library. The processing modules which include the alignment marks were strategically placed to ease the task of mask alignment. To study parameter variations across NIST9, a test module was designed and placed such that the data will be very comprehensive.

Section 8 presents the conclusions.

The test library (from which NIST8 and NIST9 were derived) contains modules that can be used to:

1. Monitor a CMOS or SOI process
2. Extract device or circuit parameters
3. Compare parameters from different device and circuit designs
4. Evaluate a CMOS or SOI process
5. Compare different CMOS and/or SOI processes via correlation coefficients and wafer maps which yield conclusions for future designs and processes.

For information on obtaining this test library, NIST8, NIST9, and the SOI/SIMOX technology file, please contact:

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For easier interpretation of the test structures, this author can be contacted for the supplement to this document [9] which is available in color.

## 2. The NIST9 SOI/SIMOX Process

NIST9 was designed for a robust NIST SOI process using SIMOX which has a 0.15  $\mu\text{m}$  silicon layer. The processing sideviews for the 14 mask steps are shown in Appendix A. Below is a list of these processing masks used to fabricate NIST9, in the order in which they are used, with the added distinction of clear or dark field:

1. Island (clear field mask)



2. *N*well/*n*-channel implant (dark field mask)
3. *P*well/*p*-channel implant (dark field mask)
4. *N*-channel MOSFET source-to-channel tie implant (dark field mask)
5. *P*-channel MOSFET source-to-channel tie implant (dark field mask)
6. Depletion-implant (dark field mask)
7.  $N^+$ poly gate implant (dark field mask)
8.  $P^+$ poly gate implant (dark field mask)
9. Polysilicon (clear field mask)
10. Source/drain  $n^+$ -implant (dark field mask)
11. Substrate contact or subcon (dark field mask)
12. Source/drain and substrate  $p^+$ -implant (dark field mask)
13. Contacts (dark field mask)
14. M1 (clear field mask)

Of the 14 processing masks specified above the following are implant masks:

1. *N*well/*n*-channel implant
2. *P*well/*p*-channel implant
3. *N*-channel MOSFET source-to-channel tie implant (also called the *ntie* implant)
4. *P*-channel MOSFET source-to-channel tie implant (also called the *ptie* implant)
5. Depletion-implant (*d*-implant)
6.  $N^+$ poly gate implant
7.  $P^+$ poly gate implant
8. Source/drain  $n^+$ -implant
9. Source/drain and substrate  $p^+$ -implant

In the next section, 2.1, the implant doses and energies chosen for these nine implantations are specified. Section 2.2 presents the rationale behind the processing sequence and mask selection in order to realize depletion-mode MOSFETs, lateral bipolar devices, and CMOS MOSFETs with source-to-channel ties.

## 2.1 Implant doses and energies for the SIMOX process

Nine implantations are used in the processing of NIST9. Five of these are *n*-type phosphorus implants, and four are *p*-type boron implants. The primary target for all of these implants is the SOI/SIMOX silicon island (which has a typical thickness of  $0.15\ \mu\text{m}$ ) except for the *npoly* and *ppoly* implants which are targetted for the CVD deposited polysilicon (which has a typical thickness of  $0.50\ \mu\text{m}$ ).

The implantation energies were chosen such that the peak concentration is placed half way into the implanted medium. This ensures that the devices are fully depleted and that the doping concentration is uniform throughout. The implanted energies listed in table 1 were selected based on the tables in reference [10]. These energies were slightly altered due to processing equipment limitations. It is possible to redesign the process formula to accomodate thicker or thinner silicon thicknesses which will allow for either a partially or fully depleted technology.

For the fabrication of NIST9, the *n*well and *p*well doses were chosen to yield threshold voltages of approximately 0.8 volts using  $n^+$  and  $p^+$  polysilicon gates for the *n*- and *p*-channels, respectively.

The channel dose for the *n*-channel depletion-mode MOSFETs was chosen to be approximately twice the well doping, a sufficient dose to overcome the pre-existing *p*well implant and sufficient to fully deplete it.

The doses for the *n*- and *p*-source/drain implantations were chosen to be  $3.0 \times 10^{15} \text{ cm}^{-2}$ .

The dose of the *ptie* (*ntie*) implant was chosen to be approximately midway between the dose of the *n*well (*p*well) implant and that of the *n*-implant (*p*-implant). The *ptie* (*ntie*) implant, as well as being the source-to-channel tie for the *p*-channel (*n*-channel) MOSFETs, doubles as the base implant of the bipolar *npn* (*pn**p*) device. The dose chosen is midway between the dose of the collector which uses the *n*well (*p*well) implant and the dose of the emitter which uses the *n*-implant (*p*-implant). This helps ensure that proper bipolar action occurs. Also, this dosage is sufficient to electrically tie the source to the channel within a diode drop. (The ties eliminate the need for an extra contact, thereby conserving silicon area.)

The doses for the *npoly* (*ppoly*) implant were considered standard at  $5.0 \times 10^{14} \text{ cm}^{-2}$ .

## 2.2 Processing sequence for NIST9

The mask sequence used to fabricate NIST9 is specified in table 2. Because of the additional structures (*n*-channel depletion-mode MOSFETs, lateral bipolar devices, and MOSFETs with source-to-channel ties) included on NIST9 (which were not included on NIST3 and NIST4), several additional masks are required, and the following issues need to be addressed:

1. How should the *ntie*, *ptie*, and d-implants be ordered ?
2. How should the *npoly* and *ppoly* implants be ordered ?
3. How should the substrate contacts be handled to avoid step coverage problems ?
4. How should the *p*-implant be ordered ?
5. Are lateral bipolar devices possible ?

With respect to the first issue, in order to electrically tie the source to the channel, the source-to-channel ties (or implants) must occur before the polysilicon deposition and after the well implants. Also, the d-implant needs to occur within these bounds. The order of these three implants (*ntie*, *ptie*, and d-) is not critical.

The structures in the test library are designed to improve circuit performance by doping the polysilicon gate with the same doping as the source and drain [11-13]. Therefore, the *npoly* and *ppoly* implants are included in the processing immediately after the polysilicon film deposition, yet before the polysilicon patterning (see table 2).

With respect to the third issue, the substrate contacts were designed to improve step



coverage by bringing the metal down to the substrate in two steps as opposed to one large step. The first contact opening to the substrate (using the subcon mask) is large ( $30\text{ }\mu\text{m}$ ), and the second contact opening (using the contacts mask) hole is smaller ( $14\text{ }\mu\text{m}$ ).

The *p*-implant occurs after the substrate contact definition (subcon). The substrate contacts are designed for use with a *p*-substrate or an *n*-substrate. In this work, a *p*-substrate is used and is recommended; therefore, the *p*-implant occurs after the subcon definition. The *p*-implant is placed in the substrate contact area to help create a good ohmic contact for the aluminum-to-substrate connection. If an *n*-substrate is used, the *n*-implant occurs after the substrate contact definition.

With respect to the fifth issue and following the processing sequence specified in table 2, lateral bipolar devices can be included in the design and fabrication of the test library and NIST9 with the inclusion of nine appropriately chosen and placed implants in the processing sequence. Considering the bipolar *nnp* (*pnnp*) devices, the *nwell* (*pwell*) implant can be used for the collector, the *ptie* (*ntie*) implant for the base, and the *n*-implant (*p*-implant) for the emitter. These lateral *nnp* and *pnnp* bipolar device designs are described in the next section.

### 3. Lateral Bipolar and CMOS-on-SOI Design

There are many different *n*- and *p*-channel MOSFET designs and lateral *nnp* and *pnnp* bipolar device designs included in the test library with various sizes and shapes. On NIST9, five different bipolar designs are included for the *nnp* devices and five for the *pnnp* devices; however, the figures and the discussion which follow refer only to the *nnp* devices.

In this section, the following MOSFET and bipolar device designs are described (fig. 2 can be used to discern the layers for all the designs in this guide):

1. *P*-channel MOSFET (fig. 3)
2. *N*-channel MOSFET (fig. 4)
3. Minimum-sized *n*-channel MOSFET (fig. 5)
4. Circular MOSFET (fig. 6)
5. Circular MOSFET with no channel contact (fig. 7)
6. H-gate MOSFET (fig. 8)
7. Italic H-gate MOSFET (fig. 9)
8. T-gate MOSFET (fig. 10)
9. H-gate MOSFET with source-to-channel tie (fig. 11)
10. T-gate MOSFET with source-to-channel tie (fig. 12)
11. *N*-channel MOSFET with source-to-channel tie (fig. 13)
12. Depletion-mode MOSFET (fig. 14)
13. Lateral bipolar (*nnp*) device with the base contact beside the emitter and with the emitter implant incorporating the collector and emitter (fig. 15)
14. Lateral bipolar (*nnp*) device with the base contact beside the emitter (fig. 16)
15. Lateral bipolar (*nnp*) device with the base contact below the emitter and with the emitter implant incorporating the collector and emitter (fig. 17)

16. Lateral bipolar ( $n p n$ ) device with the base contact below the emitter (fig. 18)
17. Lateral bipolar ( $n p n$ ) device as an  $n$ -channel MOSFET with the gate connected to the channel or base (fig. 19)

Figure 3 shows the basic  $p$ -channel MOSFET design found in the test library. In this figure, the gate extends beyond the island edge. This decreases the leakage around the gate.

Figure 4 shows the basic  $n$ -channel MOSFET design found in the test library. Selected MOSFET dimensions in figure 4 were decreased, resulting in the MOSFET shown in figure 5. Note that the  $n$ -channel MOSFET gates use the  $n^+$ poly gate implant, and the  $p$ -channel MOSFET gates (fig. 3) use the  $p^+$ poly gate implant.

Figure 6 is a circular MOSFET with a contact to the channel, and figure 7 is a circular MOSFET without this channel contact. These circular MOSFETs require substantial area and are more difficult to design than the basic MOSFETs. Since the gates are circular, there can be no leakage around the gate edge since there is no edge. Therefore, they are considered to be more hardened to increased levels of radiation.

Figure 8 shows an H-gate MOSFET. As the name implies, the gate is in the shape of an "H." The italic H-gate MOSFET is shown in figure 9, and the T-gate MOSFET is shown in figure 10. The H-gate MOSFET and T-gate MOSFET each with a source-to-channel tie are shown in figures 11 and 12, respectively. These source-to-channel ties eliminate the need for the channel contact which, in turn, conserves silicon area.

The implant for the source-to-channel tie for the MOSFETs has the same dopant type as the source and drain diffusion. As can be seen in figure 13 for an  $n$ -channel MOSFET with a source-to-channel tie, the  $n$ tie implants extend approximately half way into the channel area, extend beyond the island edges, and define which side of the MOSFET is the source.

Figure 14 gives an example of a typical depletion-mode MOSFET. For this structure, the depletion implant incorporates the channel area and extends  $2\text{ }\mu\text{m}$  beyond it in all directions. This  $2\text{-}\mu\text{m}$  extension occurs when the CIF (Caltech Intermediate Form) file is created.

The first lateral bipolar ( $n p n$ ) design can be found in figure 15. As can be seen in this figure, the  $n$ well implant encompasses the whole island. The  $p$ tie implant which defines the base reaches approximately half way under the polysilicon (a later step in the process). The  $n$ -implant occurs after the polysilicon patterning, is self-aligned, and goes from collector to emitter. When viewing the structure from left (collector contact) to right (emitter contact), the collector starts off heavily  $n$ -doped until it reaches the gate when the true collector is simply  $n$ well. The base edge which is located half way under the polysilicon is  $p$ -type ( $p$ tie). On the other side of the polysilicon, the  $n$ -implant overwhelms the  $p$ tie implant to become the emitter which completes the first lateral  $n p n$  bipolar device design. In this design, the base width is approximately half the width of the polysilicon. To design the  $n p n$  ( $p n p$ ) lateral bipolar devices, the Magic layer etch ( $p$ etch) was created (see table 3),

enabling the vertical construction of island, *nwell*, *ndiff*, *npoly*, and *poly* (island, *pwell*, *ppdiff*, *ppoly*, and *poly*).

The second bipolar (*npn*) design can be found in figure 16. It is similar to the previous design except, instead of starting at the collector contact, the *n*-implant starts on top of the polysilicon and encompasses the emitter. The collector contact does have *n*-implant inside it for a good ohmic contact to the *nwell* island, but the implant does not extend to the polysilicon in this case.

The third bipolar (*npn*) design shown in figure 17 is similar to the first design shown in figure 15 except the base contact is below the emitter contact (assuming the top of the figure is considered the top and the bottom of the figure is considered the bottom). Similarly, the fourth bipolar (*npn*) design shown in figure 18 is similar to the second design shown in figure 16 except the base contact is below the emitter contact.

The fifth bipolar design can be found in figure 19. This is an *n*-channel MOSFET with the gate connected to the channel or base.

#### 4. Updated SOI/SIMOX Technology File

Magic is the VLSI layout editor used to design the test library, NIST8, and NIST9. It includes a technology file which allows the user to modify it according to their needs. It specifies the layers, their interaction, the design rules, and the layer selection for each mask. The design rules are similar to those used to design NIST3 and NIST4 [2]. An abbreviated version of the SOI/SIMOX technology file used to design the test library, NIST8, and NIST9 is given in Appendix B.

Table 4 is a brief reference table that indicates which Magic layers correspond to which mask for NIST9. It allows one to obtain this information without sorting through the technology file. Table 5 yields this information for NIST8.

The main differences between the current SOI/SIMOX technology file and the one used to build SOI/SIMOX test chips NIST3 and NIST4 [2,3] in order to fabricate depletion-mode MOSFETs, lateral bipolar devices, and CMOS MOSFETs with source-to-channel ties are:

##### 1. The addition of the following Magic layers:

- a. *Ntie* - this implant is done before the polysilicon deposition, and it has the effect of electrically tying the channel potential to within a diode drop of the source potential for an *n*-channel MOSFET. This implant also doubles as the base implant for the lateral bipolar *pnp* devices.
- b. *Ptie* - this implant is done before the polysilicon deposition, and it has the effect of electrically tying the channel potential to within a diode drop of the source potential for a *p*-channel MOSFET. This implant also doubles as the base implant for the lateral bipolar *npn* devices.
- c. *Dimplant* - the d-implant (depletion-mode implant) was included for the construction of *n*-channel depletion-mode MOSFETs.
- d. *Dfet* - the dfet (depletion-mode MOSFET) was added to the Magic



technology file to distinguish between the different MOSFETs on the CAD system. The dfet layer implies that there is dimplant underneath this polysilicon gate.

- e. *Ppoly* - this implant layer was added so that the polysilicon can be implanted with boron for improved performance of the *p*-channel MOSFETs [11-13].
  - f. *Npoly* - this implant layer was added so that the polysilicon can be implanted with phosphorus. Poly was the Magic layer used for NIST3 and NIST4. If poly (or *npoly*) is specified for NIST9, it implies that this polysilicon will be implanted with phosphorus.
  - g. *Ppc* - this contact (*ppoly* contact) is the *ppoly*-to-metal1 contact which is specified whenever *p*-implanted polysilicon is to contact metal1.
  - h. *Pc* - this contact (poly contact) is the *npoly*-to-metal1 contact which is specified whenever *n*-implanted polysilicon is to contact metal1.
  - i. *Etch* - this layer was added to the Magic technology file in order for Magic to place *n*-doped polysilicon over *ndiff*, *nwell*, and island. This polysilicon, which is implanted with phosphorus, is used as a shield for the *npn* bipolar devices and can be etched away after the *p*-implant if desired.
  - j. *Petch* - this layer was added to the Magic technology file in order for Magic to place *p*-doped polysilicon over *ppdiff*, *pwell*, and island. This polysilicon, which is implanted with boron, is used as a shield for the *pnp* bipolar devices and can be etched away after the *p*-implant if desired.
  - k. *Open* - if this layer is specified, the raw silicon substrate will be exposed to air after processing such that during the post-processing anisotropic etch, the silicon can be etched away. This etching (or micromachining) is done to realize suspended structures [14].
  - l. *Hole* - this layer appears only on the contact mask. This opening in the oxide is used in the SIMS (secondary ion mass spectroscopy) structures to facilitate the measurement of doping densities on modules AAM5 and AAM6.
  - m. *Legend* - this layer was added to the technology file to aid in labeling the pads for probing purposes. This layer does not appear in the CIF file.
  - n. *Legend\_background* - this layer was added to the technology file to aid in rapidly placing the labels within the pads. This layer does not appear in the CIF file.
2. The layer "pad" is used to specify a bond pad. Its dimensions (before CIF) are 112  $\mu\text{m}$  by 112  $\mu\text{m}$  in the test library, and the layer dimensions (after CIF) for NIST9 are:
- a. Island (112  $\mu\text{m}$   $\times$  112  $\mu\text{m}$ )
  - b. Polysilicon (108  $\mu\text{m}$   $\times$  108  $\mu\text{m}$ )
  - c. *Npoly* implant (108  $\mu\text{m}$   $\times$  108  $\mu\text{m}$ )
  - d. Contact (92  $\mu\text{m}$   $\times$  92  $\mu\text{m}$ )

- e. Metall (104  $\mu\text{m}$   $\times$  104  $\mu\text{m}$ )

The pad layer dimensions (after CIF) for NIST8 are:

- a. Polysilicon (112  $\mu\text{m}$   $\times$  112  $\mu\text{m}$ )
  - b. Metall (108  $\mu\text{m}$   $\times$  108  $\mu\text{m}$ )
  - c. Polycontact (106  $\mu\text{m}$   $\times$  106  $\mu\text{m}$ )
  - d. Metall (104  $\mu\text{m}$   $\times$  104  $\mu\text{m}$ )
  - d. M2c (102  $\mu\text{m}$   $\times$  102  $\mu\text{m}$ )
  - e. Glass (100  $\mu\text{m}$   $\times$  100  $\mu\text{m}$ )
3. For the layer "ppad," all the above layers in item 2 for NIST9 are included except the layer "ppoly implant" replaces "npoly implant" with the same dimensions. Ppad is used to specify a bond pad whenever *p*-implanted polysilicon is used to make the pad connection.
  4. The substrate contact is treated differently and must be designed differently to obtain working contacts. Additional information can be found in the section called "Processing Sequence for NIST9."

## 5. Test Library

New test chips can be custom designed from the modules in the test library or the modules can be used as "drop-in's." From the test library, test chip NIST8 and test wafer NIST9 were built. A module is a single (or group of) test structure(s) which can be tested by the single positioning of one set of probes. There are five different sizes of modules (i.e., five different probe pad configurations); however, each module can be considered small, medium, or large depending on the sizes of MOSFETs chosen within the module. (There are five different probe pad configurations, but only one or two different probe cards are needed for testing.)

Figure 20 shows the outline of the test library with the corresponding possible module count given the existing organization. There are 686-2 by 16 modules, 130-12 by 2 modules, 90-10 by 7 modules, 72-10 by 2 modules, and 22-2 by 11 modules. This results in a total of 1000 modules, given the layout of modules shown whose area is equivalent to a quarter of a 10.16-cm (4-in.) wafer. (A 2 by 16 module implies there are 2 columns and 16 rows of probe pads. This naming convention is true for all the other modules except for the 10 by 7 module. For this module there are 10 pads along the top, 10 pads along the bottom, 7 pads along each side, and the middle area is for circuitry.)

The five different module sizes shown in figure 20 are given in table 6. All the probe pads have a 200- $\mu\text{m}$  center-to-center spacing. The cell nomenclature for these modules is also included in this table. For example, a 12 by 2 module could be called "aaS," "ooM," "qcL," etc.

The five different module types given in table 6 can be small, medium, or large depending on the MOSFET sizes chosen (the pad arrangements and module dimensions remain the same). The cell names of the small modules end with an "S," the names for the medium modules end with an "M," and for the large modules the cell names end with an "L." The



lower portion of table 6 gives the nominal MOSFET dimensions for the small, medium, and large 2 by 16 modules along with a sample subcell name which is descriptive of the MOSFET's dopant type, design, and channel dimensions.

To convert a medium module into a small module, the procedure is given in table 7. This is a difficult task involving submicrometer dimensions and, therefore, grid alterations. It is the last thing that is done because a .mag file magnified by a factor of 10 is needed to design using submicrometer dimensions. Therefore, after the entire wafer is designed except for the submicrometer dimensions, a CIF file is generated and read back in an order of a magnitude larger. The submicrometer dimensions are then designed into the file while considering the scale factor. The CIF file is created using a scale factor which reduces the design by a factor of 10 and is sent to the mask makers. This resulting .cif file will retain the submicrometer character of the design; however, if this file is read back into Magic without magnification, the submicrometer dimensions will be rounded to the nearest micrometer and any .cif file generated by this .mag file will exhibit the rounded numbers and not the submicrometer dimensions. Therefore, creating the submicrometer dimensions should be the last thing that is done before submitting a design to the mask makers.

The 2 by 16 module is defined to be the basic module. Given a 2 by 16 probe pad arrangement with a center-to-center pad spacing of  $200\text{ }\mu\text{m}$ , it is possible to fit a MOSFET with a channel area of  $50\text{ }\mu\text{m}$  by  $50\text{ }\mu\text{m}$  between these pads. Any pad spacing larger than  $200\text{ }\mu\text{m}$  would result in a lot of unused silicon area. Inside a 2 by 16 module, it is possible to put six MOSFETs with individual connections to the source, gate, drain, and channel. For this work, the substrate contact connections can be shared with neighboring MOSFETs. Each of the six MOSFETs within the 2 by 16 module has different channel dimensions. Also, the pad dimensions are large enough ( $112\text{ }\mu\text{m}$  by  $112\text{ }\mu\text{m}$ ) such that they can be wire bonded (exposed metal area on NIST9 is  $104\text{ }\mu\text{m}$  by  $104\text{ }\mu\text{m}$ ). Individual packaged modules are also possible for these narrow 2 by 16 modules [15].

The final wafer or chip can be separated using a wafer saw. The 2 by 16 modules are placed next to each other conserving the  $200\text{-}\mu\text{m}$  center-to-center pad spacing. If the modules are separated, the narrow-bladed saw will pass through the center of the neighboring 2 by 16 modules. These sacrificed modules can be probed beforehand, or they can be duplicated on the chip or wafer.

The large 10 by 7 modules are needed because most circuits will not fit within the 2 by 16 probe-pad arrangement. A circuit could be placed to the right of a 2 by 16 probe-pad arrangement with the wiring routed to the appropriate pads; however, if these circuits are to be irradiated, the probes will shield parts of the circuit from the radiation while it is being tested. Therefore, the large 10 by 7 modules have 30 pads along the periphery (including the corners). There are 10 pads located along the top, 10 pads along the bottom, and 7 pads on each side.

The remaining three module types are sacrificial modules used adjacent to the 2 by 16 modules and/or the large 10 by 7 modules. As shown in figure 20, the horizontal 12 by 2 modules are placed above and below the 2 by 16 modules. If a 2 by 16 module is packaged,

the 12 by 2 modules will be sacrificed on the ends, thus keeping intact the 2 by 16 modules above and below the one to be packaged. In addition to the 12 by 2 modules, the 10 by 2 horizontal modules are used as the sacrificial modules above and below the large 10 by 7 modules. These large 10 by 7 modules were arranged together, in this case along the bottom, to minimize the sawing task. And the remaining 2 by 11 modules are placed along the bottom row of large 10 by 7 modules. The module arrangement is highly versatile. Perhaps it is desired to package the horizontal (12 by 2 or 10 by 2) modules in which case a different approach to module placement is recommended.

Figure 21 shows the module spacings for the various modules. The module-to-module spacing occurs in multiples of 200  $\mu\text{m}$  due to the center-to-center probe-pad spacing of 200  $\mu\text{m}$ . This facilitates the placement of modules.

All MOSFETs are oriented in the same way for ease in testing. That is, the gate is the upper left-hand probe pad, the drain is the upper right, the source the lower left, and the channel is the lower right-hand probe pad. For a *p*-type substrate, the substrate connection will be either the pad directly above the drain pad or the pad directly below the channel pad depending upon the MOSFET's location within the 2 by 16 module arrangement. For an *n*-type substrate, the substrate connection is either the pad directly above the gate pad or the pad directly below the source pad. Given the MOSFET's location within the 2 by 16 module arrangement, the substrate connections will be in the same place on other 2 by 16 MOSFET modules. Figure 21 gives the MOSFET and substrate contact locations for four of the five module types which have a different number of probe pads and, therefore, can accommodate a different number of MOSFETs and substrate contact arrangements. (MOSFETs are not routinely pinned out on the large 10 by 7 modules since they fit in a more reasonable space on the other four module types.)

Table 8 lists the large 10 by 7 modules that are available in the test library. This list for the 2 by 16 modules, and the other miscellaneous modules is found in table 9. A listing of the large 10 by 7 modules in table 8 organized by function is given in table 10 with a comparable list of the modules in table 9 given in table 11. These lists are further subdivided into tables 12 through 16 which list the different MOSFETs, meanders, capacitors, and dynamic circuits.

## 6. Test Chip NIST8

To compare and contrast bulk CMOS and SOI processes, test chip NIST8 was constructed from various modules in the test library. It is a CMOS-on-SOI design that was converted to a CMOS on bulk silicon design via the technology file given in Appendix B. The CIF file created by Magic's technology file was submitted to MOSIS for fabrication on a 2.0- $\mu\text{m}$  ( $\lambda=1.0$ ) processing run. An *n*well process was used; however, a *p*well process would have resulted in working parts as well.

The size of NIST8 ( $x=4410\ \mu\text{m}$ ,  $y=6800\ \mu\text{m}$ ) was chosen to accommodate fabrication by MOSIS. NIST8 is composed of four large 10 by 7 modules, twelve 2 by 16 modules, one 12 by 2, and three 10 by 2 modules. Figure 22 shows the cell structure of NIST8, figure 23 shows the subcell structure of NIST8, and table 17 includes the dopant type and device



sizes on a row and column basis. Figure 24 shows the actual layout of NIST8. The 2 by 16 modules on NIST8 include:

1. Module AM - *N*-channel MOSFETs (with various lengths and widths) (see fig. 4)
2. Module BM - *P*-channel MOSFETs (with various lengths and widths) (see fig. 3)
3. Module CM - Minimumly designed *n*-channel MOSFETs (see fig. 5)
4. Module DM - Circular *n*- and *p*-channel MOSFETs with a well contact (see fig. 6)
5. Module KM - Circular *n*- and *p*-channel MOSFETs without a well contact (see fig. 7)
6. Module EM - H-gate MOSFETs (see fig. 8)
7. Module UM - Italic H-gate MOSFETs (see fig. 9)
8. Module FM - T-gate MOSFETs (see fig. 10)
9. Module VM - Inverters
10. Module XM - Alignment structures
11. Module AaM - Square *n*-channel MOSFETs
12. Module BbM - Square *p*-channel MOSFETs

The large 10 by 7 modules include:

1. Module DDM - An SRAM (see fig. 25)
2. Module EEM - A 23-stage ring oscillator using regular MOSFETs (see fig. 26)
3. Module GGM - A 23-stage ring oscillator using H-gate MOSFETs (see fig. 27)
4. Module OOM - Large *n*-channel MOSFETs for radiation investigations (see fig. 28)

And the horizontal modules include:

1. Module aaM - *N*-channel MOSFETs
2. Module bbbM - *P*-channel MOSFETs
3. Module aaaM - Unusually sized *n*-channel MOSFETs
4. Module cccM - Unusually sized *p*-channel MOSFETs

In the test library, the substrate contacts are placed at strategic locations on each 2 by 16 module such that each test structure is adjacent to one. This is intended only for SOI processing. For the CMOS processing of NIST8, the "substrate" connections disappear after a CIF file is generated. In other words, what was a substrate contact, becomes metal and *p*-implant, the construction of which has no purpose in CMOS. The pads labeled "W" for "well" on NIST8 are used to bias the CMOS devices which are sufficient to probe the MOSFETs and circuits on NIST8.

NIST8 requires the use of submicrometer dimensions in the alignment structures on module XM. A method to obtain submicrometer dimensions on NIST8 is given in table 18. This was the last thing done before submission to MOSIS.

All of the test structures on NIST8 (excluding the ring oscillators which were probed manually) were probed using an HP 4062UX Semiconductor Process Control System. The test algorithms can be found in Appendices C through F. They perform the following:

1. the test algorithm KEYSiv (Appendix C) obtains the *IV* data points for *n*- or

- p*-channel MOSFETs,
2. KEYSvt (Appendix D) obtains the  $I_{DS}$  versus  $V_{GS}$  curves for various values of  $V_{BS}$ ,
  3. the test algorithm INV (Appendix E) obtains the  $V_{IN}$  versus  $V_{OUT}$  data for inverters, and
  4. the test algorithm SRAM (Appendix F) plots the output of the SRAM given various input stimulus.

All of these algorithms acquire data suitable for the evaluation procedure KEYS [5]. The circuit diagram of the static RAM cell (and how to test it) is given in figure 29.

An example SPICE file for the MOSFETs, inverters, regular ring oscillators, H-gate ring oscillators, and SRAM can be found in Appendices G through K. These were used in the computer procedure KEYS.

## 7. Test Wafer NIST9

SOI/SIMOX test wafer NIST9 is comprised of numerous modules taken from the test library and organized such that they would fit onto a quarter of a 10.16-cm (4-in.) wafer. This quarter-wafer constraint is to accommodate a 7.62-cm (3-in.) based fabrication facility at NIST. To maximize the use of the SIMOX wafers, the 10.16-cm (4-in.) wafers were sawed into quarters and then processed. Actually, the radius of NIST9 (if it were a whole wafer) needed to be approximately 6 mm less than 5.08 cm (2 in.) to facilitate handling and equipment constraints.

To easily align the masks, the locations for the main processing module, called AAM (the only expanded module shown in fig. 30), are critical. This module, shown in figure 31, contains the alignment marks. The alignment marks on this module are viewed and paired with the alignment marks on another AAM processing module for mask alignment. These main processing modules need to be separated by approximately 2.54 cm (1 in.). If they are much closer, the alignment microscope cannot see both modules at once, and alignment becomes a more difficult task.

The horizontal processing module AAM1 (fig. 32) appears below each main AAM module. Module AAM1's purpose is to help grossly align those masks which have a dark field.

NIST9 includes many of the modules from the test library. The placement of the modules on NIST9 (fig. 30) is similar to the module placement in the test library (fig. 20) except that more large 10 by 7 modules occupy the lower portion and right-hand portion of the wafer (without sacrificial modules surrounding them). These large 10 by 7 modules are the process monitor modules (called AAM2 through AAM6) which will be sacrificed during the processing. They include structures for the following:

1. cross sections for SEM,
2. SIMS targets for doping concentrations, and
3. MOSFETs to probe during processing.

Table 19 was used to help organize the other large 10 by 7 modules, and table 20 was used to help organize the 2 by 16 modules that are detailed in tables 8 and 9, respectively.

To study parameter variations across the wafer, the 2 by 16 module CcM was designed. This 2 by 16 module includes the following:

1. a 6- $\mu\text{m}$  polysilicon cross bridge resistor,
2. an  $n$ -channel MOSFET with  $L=6\ \mu\text{m}$  and  $W=6\ \mu\text{m}$ ,
3. a  $p$ -channel MOSFET with  $L=6\ \mu\text{m}$  and  $W=12\ \mu\text{m}$ ,
4. an inverter with  $L=6\ \mu\text{m}$ ,  $W_n=6\ \mu\text{m}$ , and  $W_p=12\ \mu\text{m}$ , and
5. a  $p$ -channel MOSFET with  $L=6\ \mu\text{m}$  and  $W=6\ \mu\text{m}$ .

This is referred to as the KEYS module in table 20 which occupies every other 2 by 16 module slot on the wafer. The MOSFETs and inverters on this module can be tested on the HP 2062UX using the test algorithms in Appendices C, D, and E. The data from these test structures can be evaluated (and wafer maps obtained) by the computer procedure KEYS. Also, the horizontal 12 by 2 module bbM includes the same structures listed above except for the  $p$ -channel MOSFET with  $L=6\ \mu\text{m}$  and  $W=6\ \mu\text{m}$ . On this horizontal module, the structures are rotated 90 deg to make horizontal and vertical parameter mapping possible.

The remaining 2 by 16 modules include the following:

1. MOSFETs - oriented such that the gate is the upper-left-hand probe pad, the drain is the upper-right-hand probe pad, the source is the lower-left, and the channel is the lower-right. The  $IV$  characteristics and threshold voltage data can be compared for the differently designed MOSFETs with the same channel dimensions. The differently designed MOSFETs include:
  - a.  $N$ - and  $p$ -channel MOSFETs (with and without source-to-channel ties)
  - b. Depletion-mode MOSFETs
  - c. Circular MOSFETs (with and without channel contacts)
  - d. H-gate MOSFETs with the same dimensions as the T-gate MOSFETs (with and without source-to-channel ties)
  - e. Italic H-gate MOSFETs
  - f. T-gate MOSFETs (with and without source-to-channel ties)
2. Contact resistors
3. Cross-bridge resistors
4. Inverters
5. E-beam X-ray alignment structures
6. Lateral bipolar  $npn$  and  $pnp$  devices

The large 10 by 7 modules are intended to be used for radiation studies. The circuitry is within the area to be bonded, and therefore, the probes will not block any incoming radiation. The large 10 by 7 modules on NIST9 include the following:

1. The processing modules
2. Large capacitors from which to obtain various capacitance values
3. Three different varieties of meanders of different types



4. Ring oscillators pinned out for a 2 by 16 or a square probe card. All the different ring oscillators use the same pinout. The different 23-stage ring oscillator modules include the following MOSFET designs:
  - a. *N*- and *p*-channel MOSFETs (with and without source-to-channel ties)
  - b. Circular MOSFETs (with and without channel contacts)
  - c. H-gate MOSFETs (with and without source-to-channel ties)
  - d. T-gate MOSFETs (with and without source-to-channel ties)
5. SRAMs using *n*- and *p*-channel MOSFETs and circular MOSFETs
6. Diodes
7. Van der Pauws (dopant resistivity devices)
8. Suspended structures including MOSFETs, diodes, resistors, and an OH breath analyzer (see fig. 33)

The OH breath analyzer (fig. 34) [16] is a micromachined structure which suspends the central trampoline-like area by the support arms. This suspension occurs after the NIST9 wafer is selectively protected with glass (which is not included in the 14-mask process) and then a post-processing anisotropic etch [14] is performed which etches away the raw silicon exposed in the designed open areas. After a sufficient amount of time in the etch solution, a large inverted pyramidal pit is formed whose rectangular base edges are adjacent to the inside dimensions of the *p*-implant, which is an effective etch stop, leaving the island with the diffused resistor mainly encompassed in oxide and suspended in air. On the right of this suspended island are contacts to the island and a glass cut covering both these contacts.

When the diffused resistor heats the suspended island up to 300 °C, if the glass opening is covered with a thin layer of bismuth, the resistance between those two contacts will change significantly in the presence of OH which can come from the breath of an intoxicated individual.

## 8. Conclusions

With the experience gained from the design, fabrication, and testing of NIST3 and NIST4 [2,3], a test library, NIST8, and NIST9 were designed to evaluate and compare CMOS test structures, including devices and circuits, fabricated on both bulk silicon and SOI/SIMOX wafers. This is the design and testing guide for the test library, NIST8, and NIST9. The test library was created from which the CMOS test chip NIST8 was designed and subsequently fabricated through MOSIS (on bulk silicon only), and the SOI/SIMOX test wafer NIST9 (a 14-mask process) was designed for fabrication at the NIST processing facility or for outside users of this design.

The processing sequence for the NIST9 SOI/SIMOX process was presented in section 2 along with the implant doses and energies chosen for the nine implantations which are optimized for fully depleted devices on 0.15  $\mu\text{m}$  silicon on buried oxide. These nine implantations made it possible to realize depletion-mode MOSFETs, lateral bipolar devices, and CMOS MOSFETs with source-to-channel ties, the designs of which are presented in section 3. Suspended structures were also designed which will require a protective glass coating (NIST9 does not have this) and a subsequent post-processing etch.

The technology file of Magic (the CAD graphic layout editor used in this work) was modified to make the design of the 14-mask SOI/SIMOX process possible. This technology file converts the CMOS and lateral bipolar SOI design of the test library into the CMOS design of test chip NIST8 and/or the SOI design of test wafer NIST9. This is done in the "cifoutput" section of the technology file.

Given the test results from NIST9, the CMOS device and circuit parameters from NIST8 can be presented and compared with the SOI device and circuit parameters from NIST9. Using the computer procedure KEYS, the parameters from the *IV* characteristics for the different MOSFET and circuit designs included on NIST8 and NIST9 can be evaluated, parameter correlation coefficients can be obtained, and parameter wafer maps can be generated, yielding conclusions for future designs and processes.

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- [16] Conversations with M. Parameswaran (micromachining expert), Simon Fraser University, Burnaby, British Columbia.

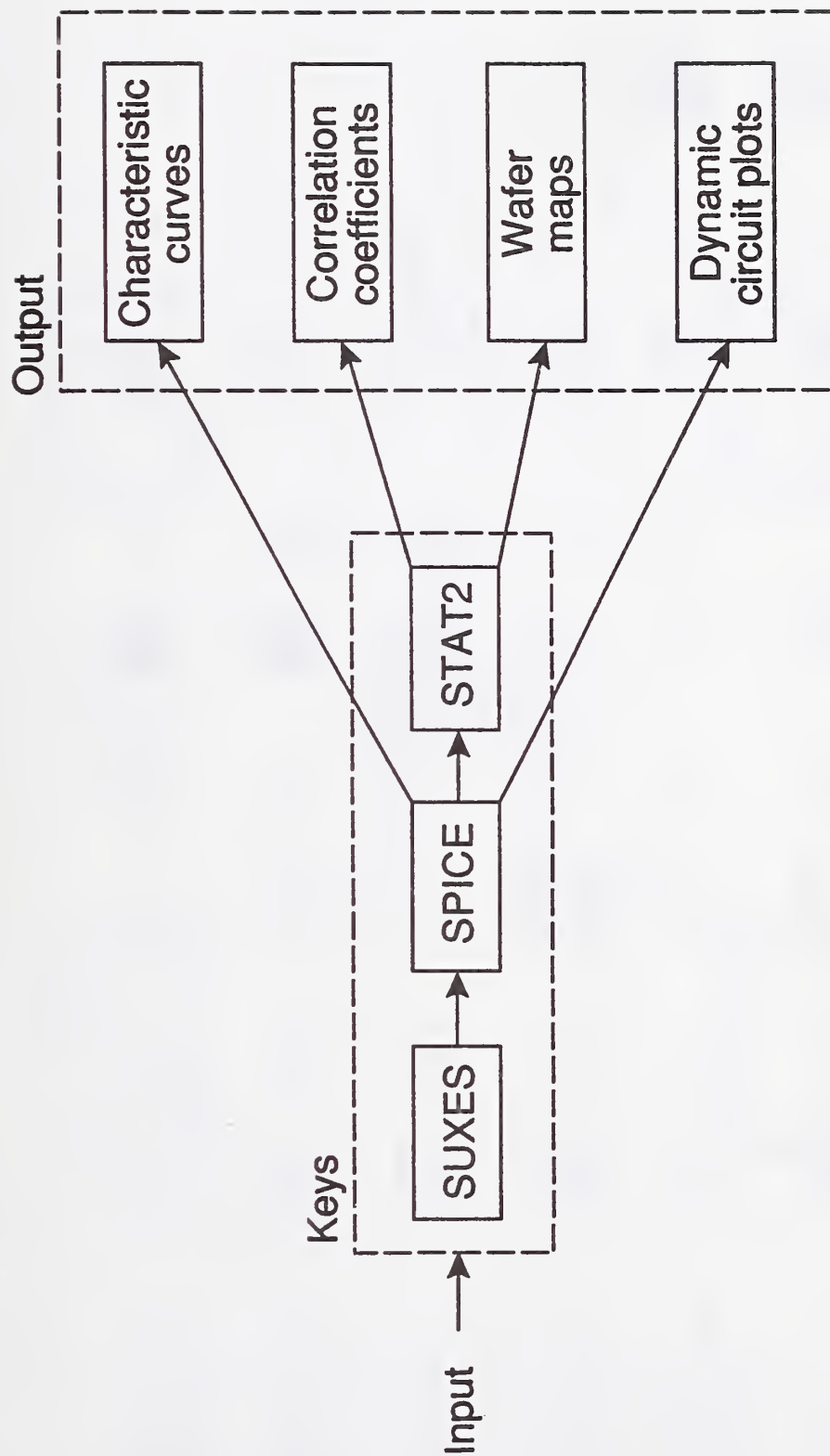


Figure 1. Simplified block diagram for the computer procedure KEYS.



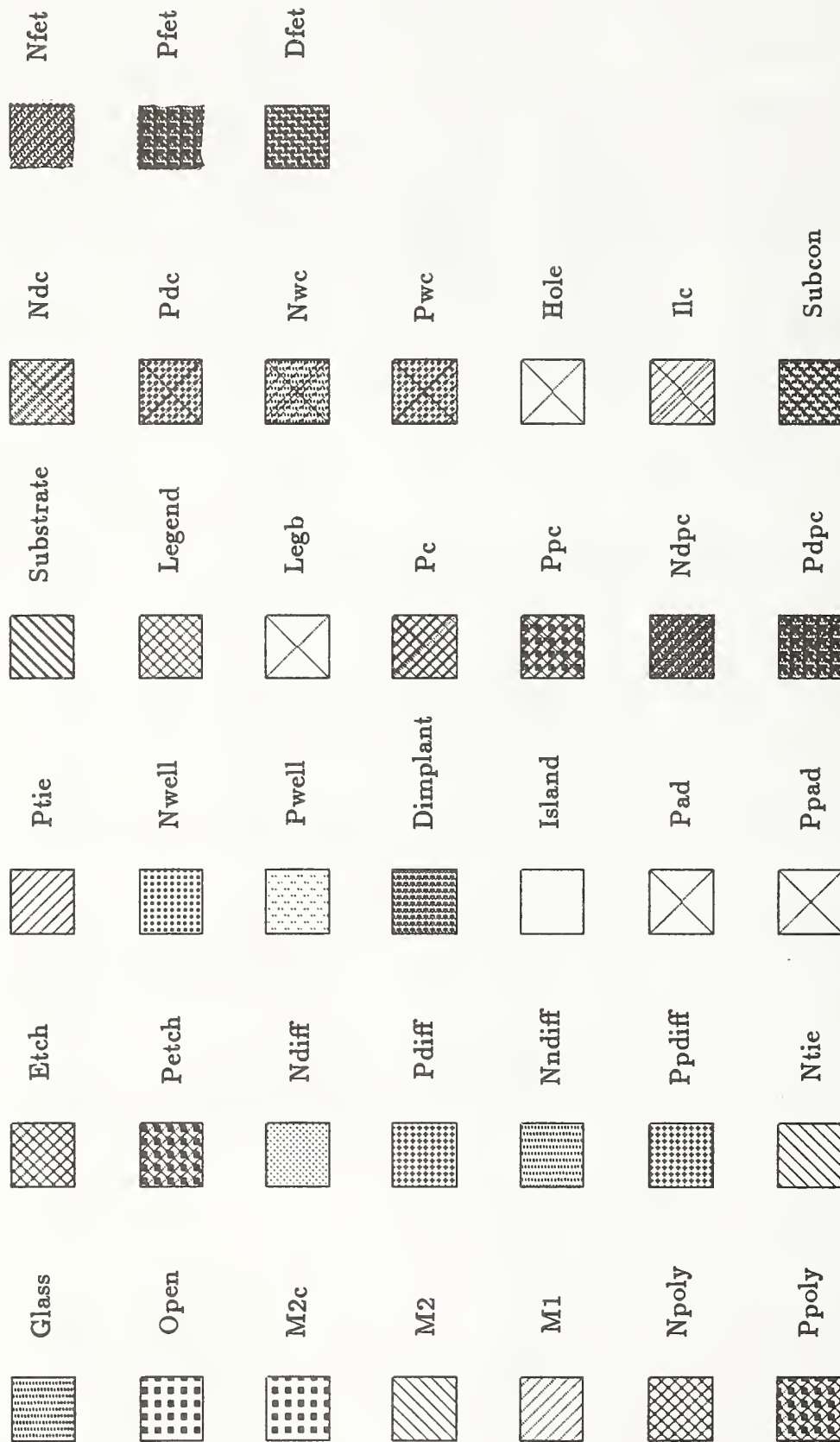


Figure 2. Key to the shading in the figures. These layers correspond to the Magic layers in the SOI/SIMOX technology file.



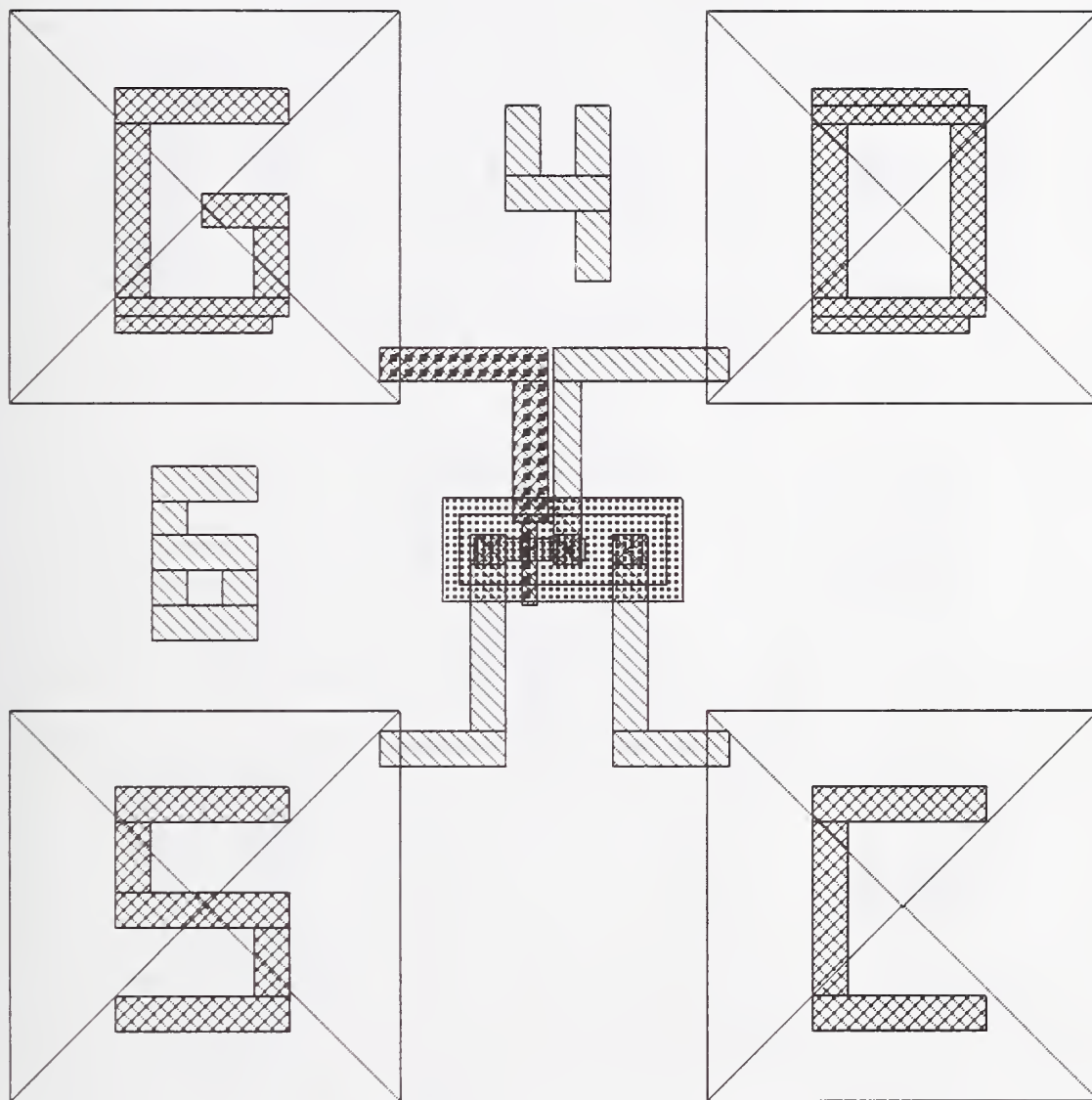


Figure 3. *P*-channel MOSFET found in the test library, NIST8, and NIST9.

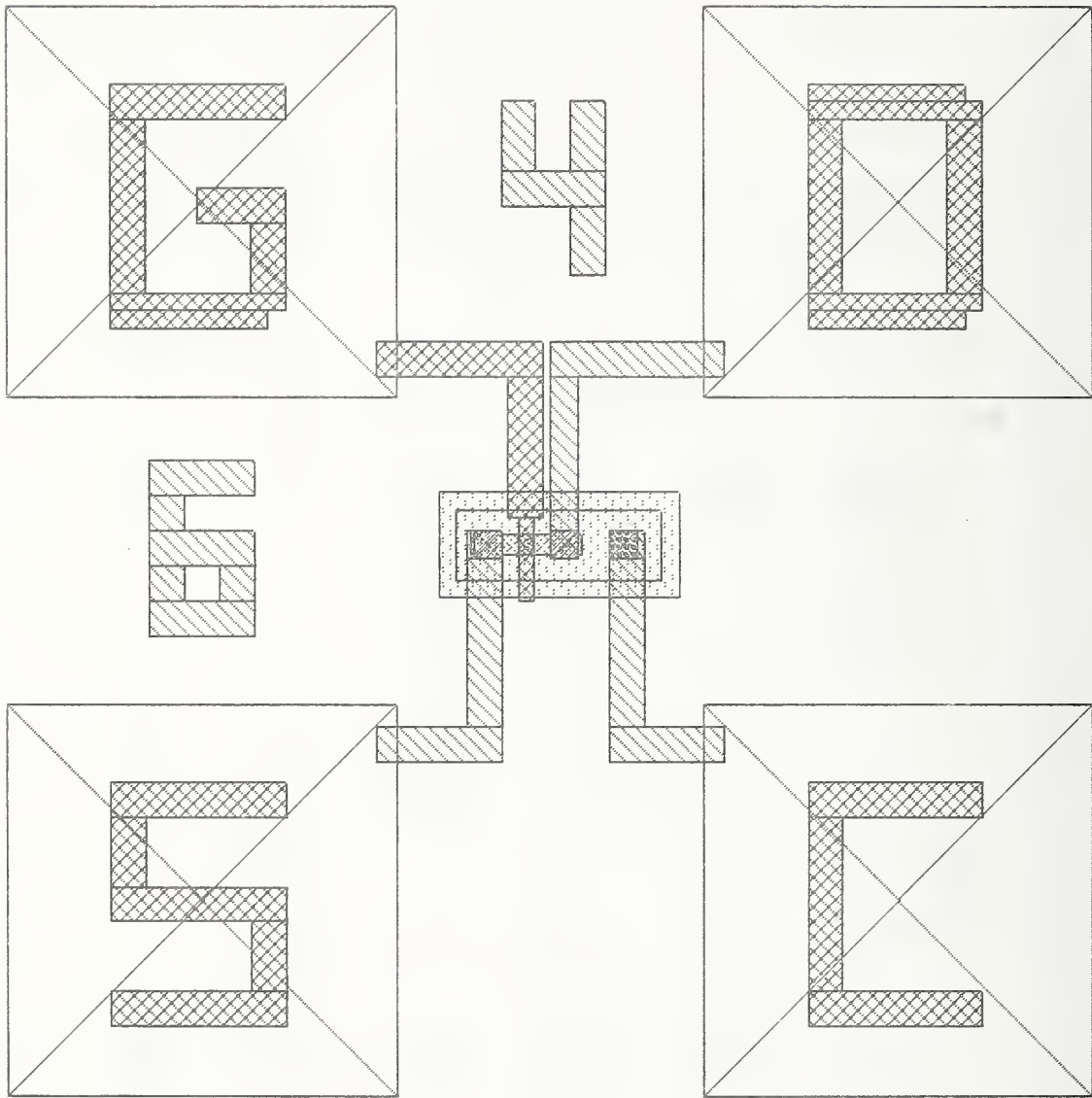


Figure 4. *N*-channel MOSFET found in the test library, NIST8, and NIST9.

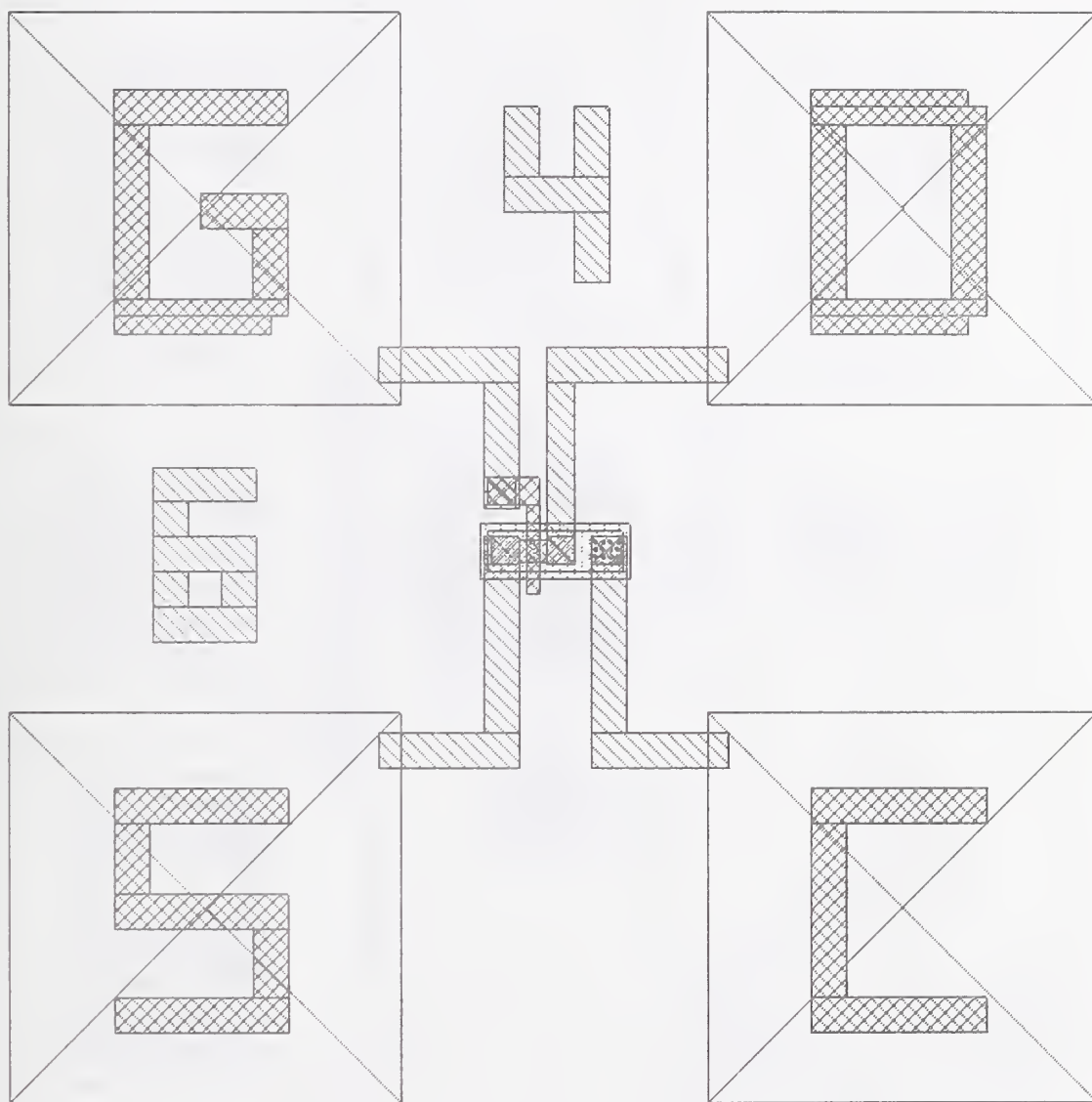


Figure 5. Minimum-sized *n*-channel MOSFET found in the test library, NIST8, and NIST9.

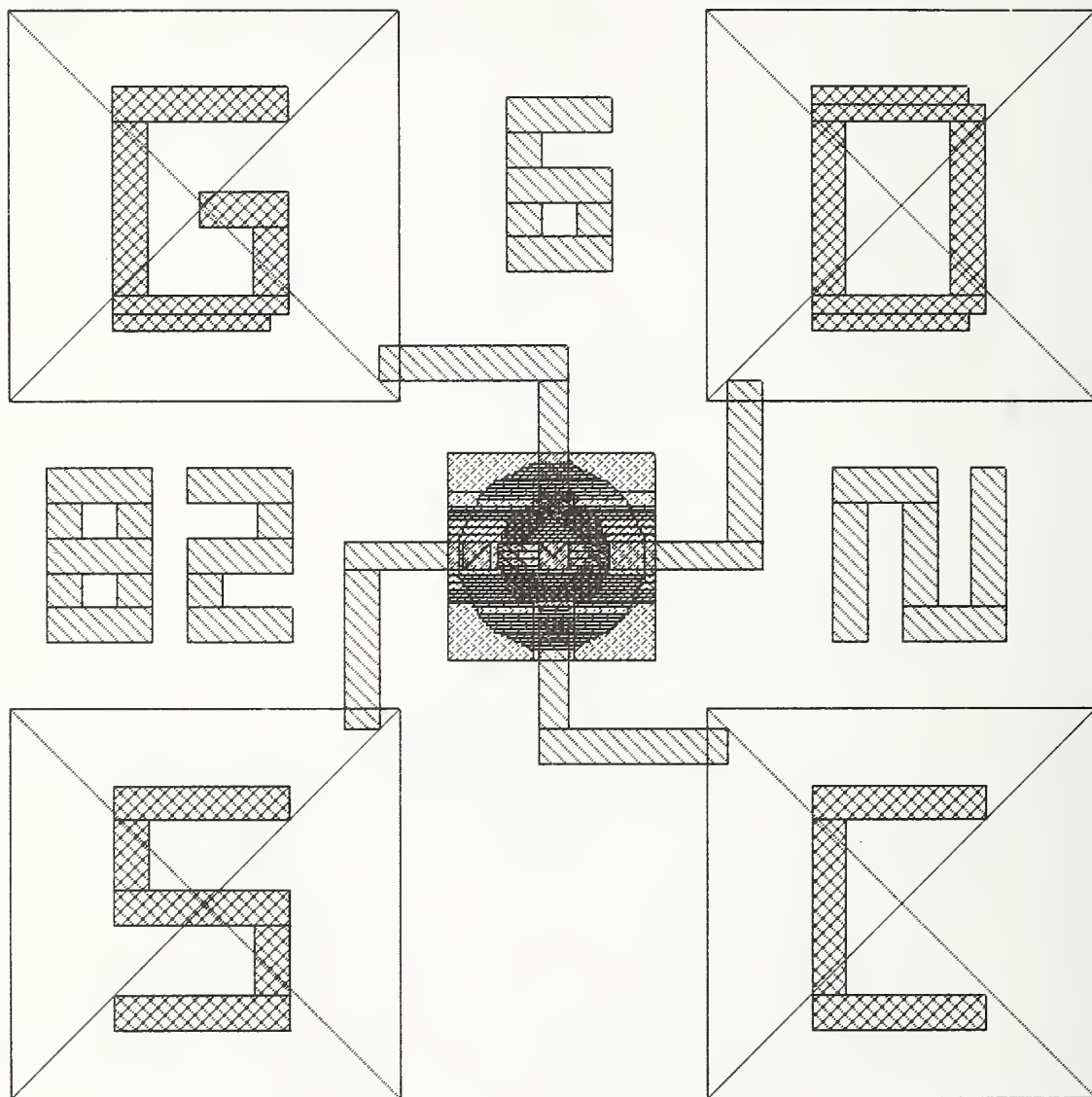


Figure 6. Circular  $n$ -channel MOSFET found in the test library, NIST8, and NIST9.



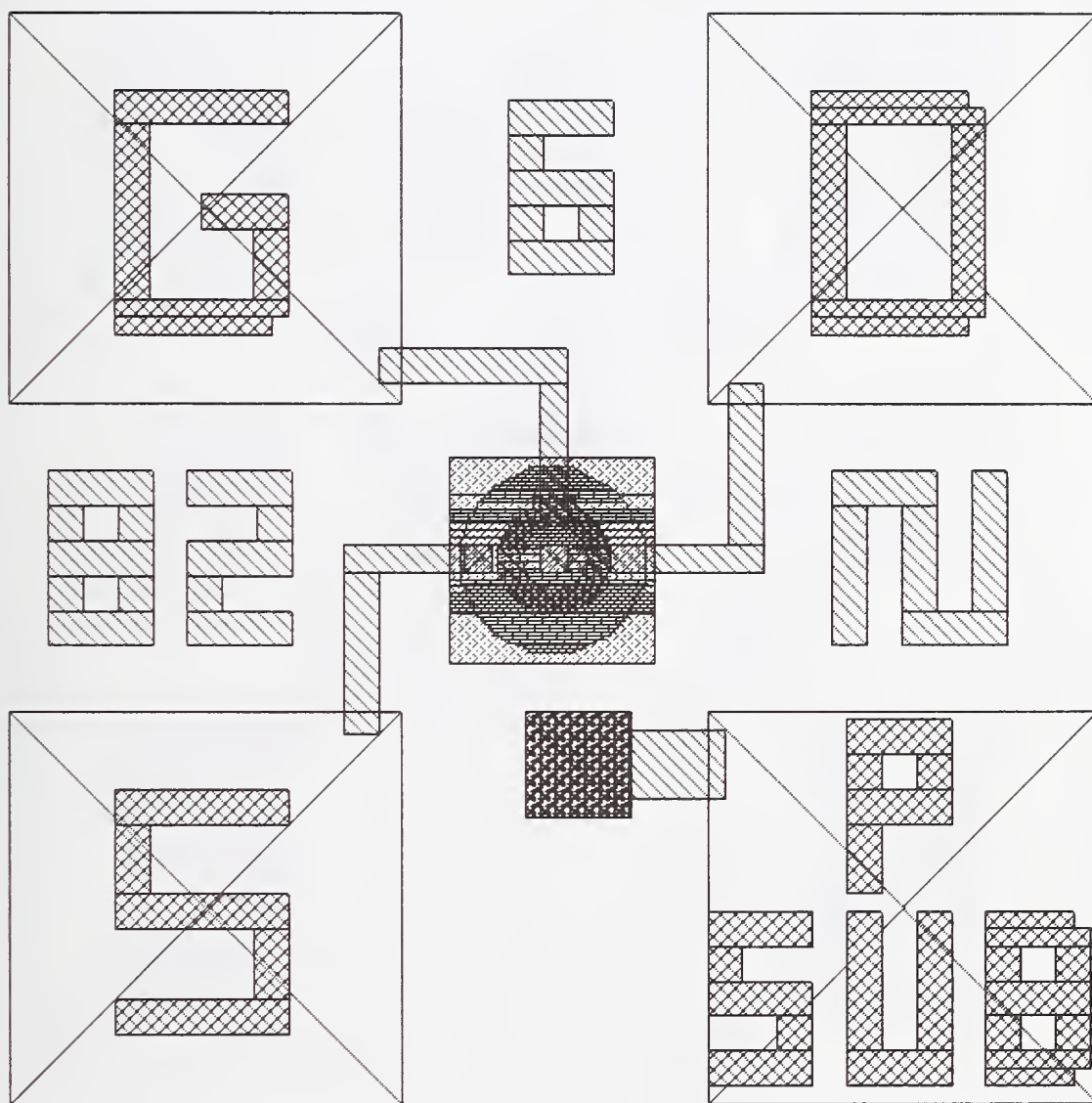
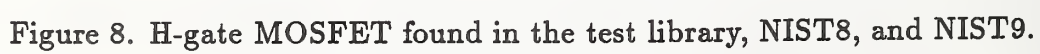


Figure 7. Circular  $n$ -channel MOSFET with no channel contact found in the test library, NIST8, and NIST9.



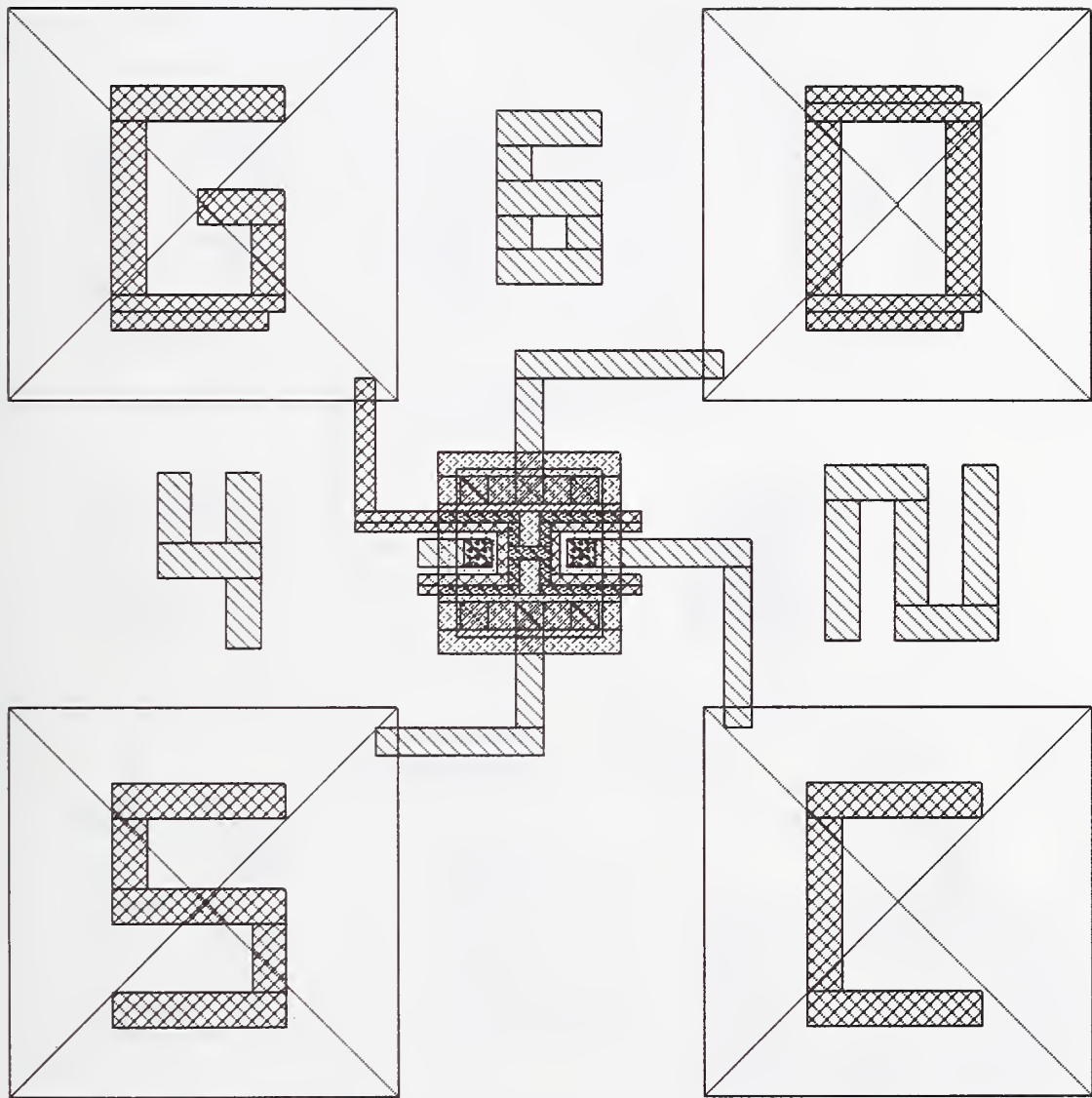


Figure 9. Italic H-gate MOSFET found in the test library, NIST8, and NIST9.



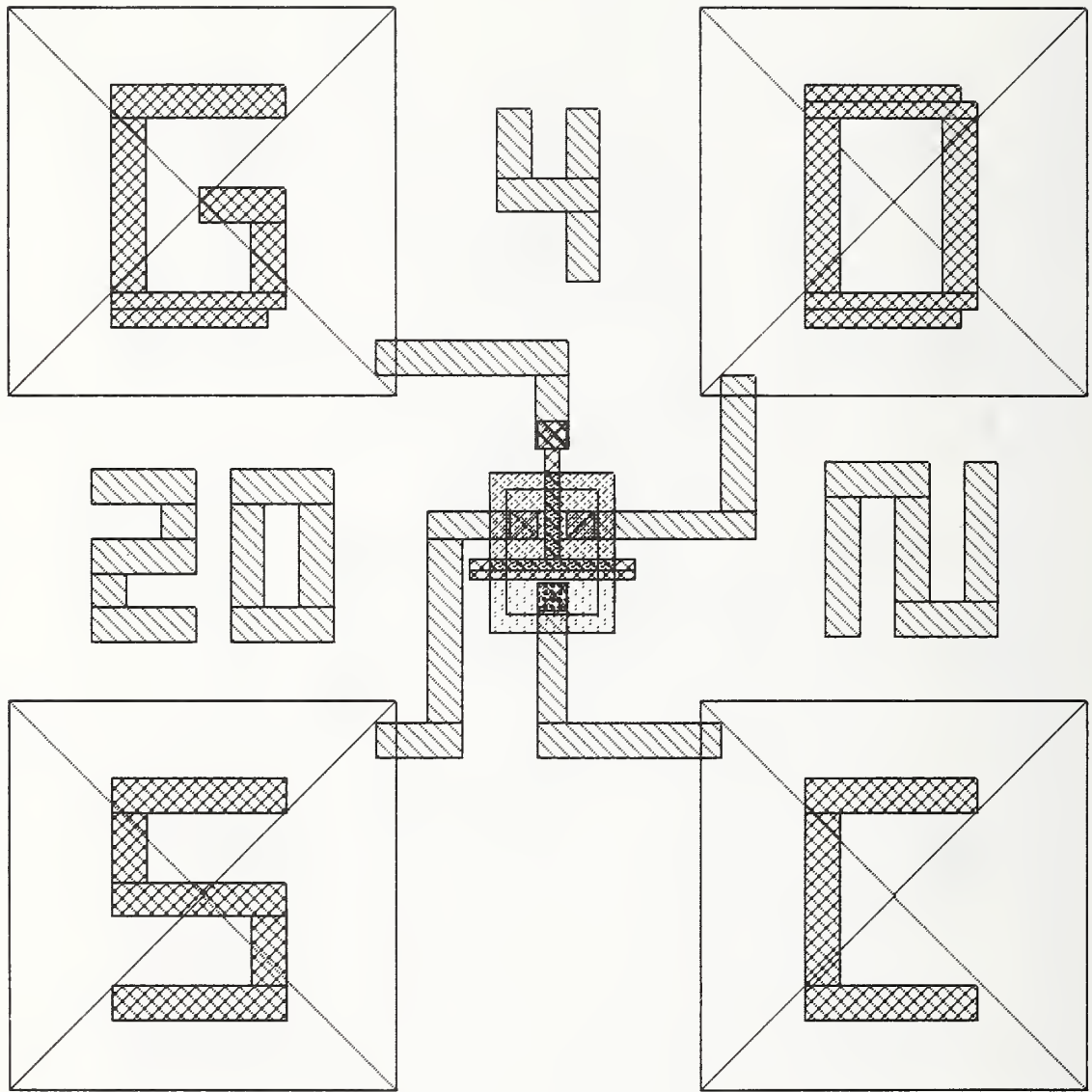


Figure 10. T-gate MOSFET found in the test library, NIST8, and NIST9.

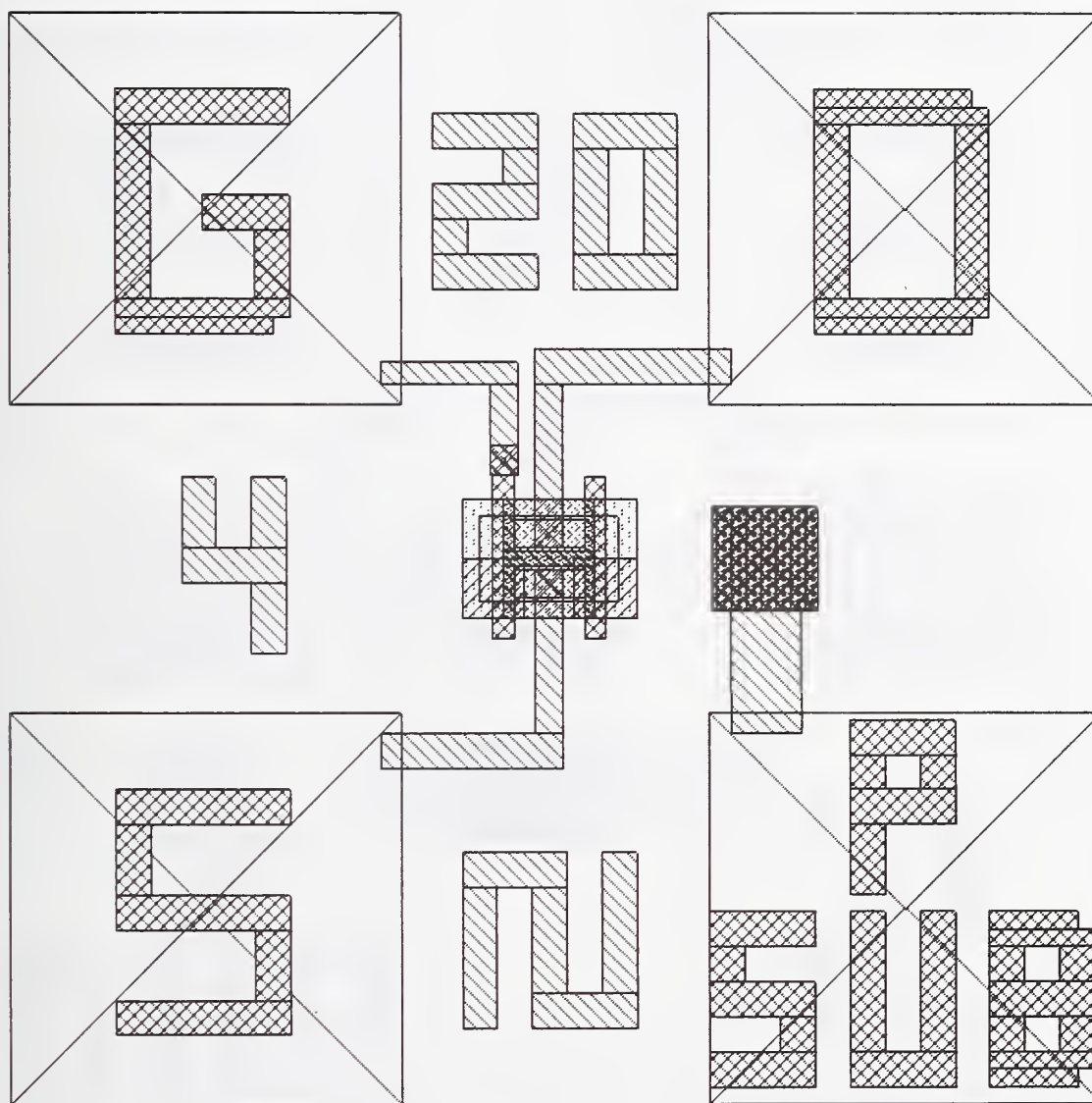


Figure 11. H-gate MOSFET with source-to-channel tie found in the test library, NIST8, and NIST9.

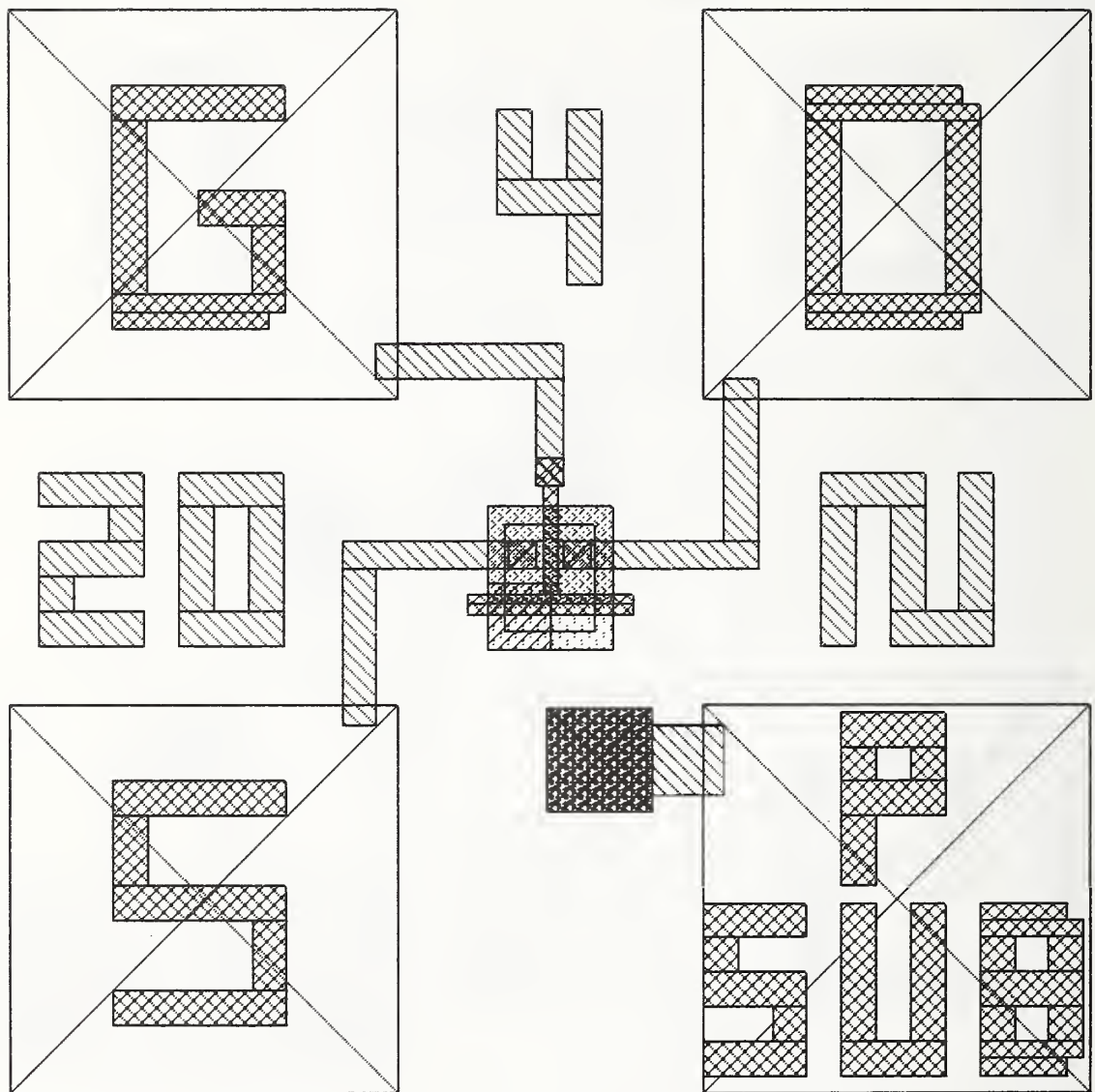


Figure 12. T-gate MOSFET with source-to-channel tie found in the test library, NIST8 and NIST9.



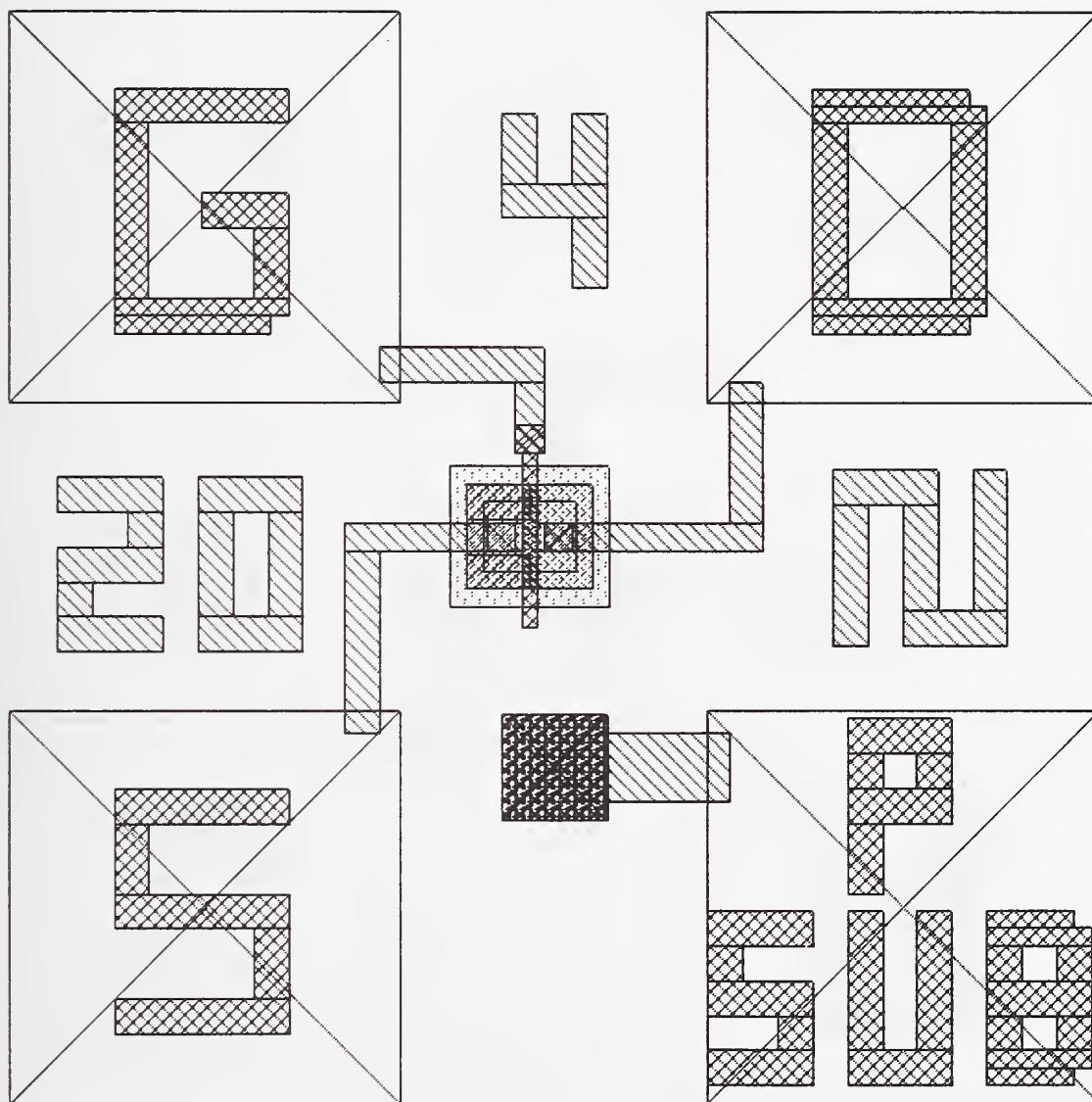


Figure 13. *N*-channel MOSFET with source-to-channel tie found in the test library and NIST9.

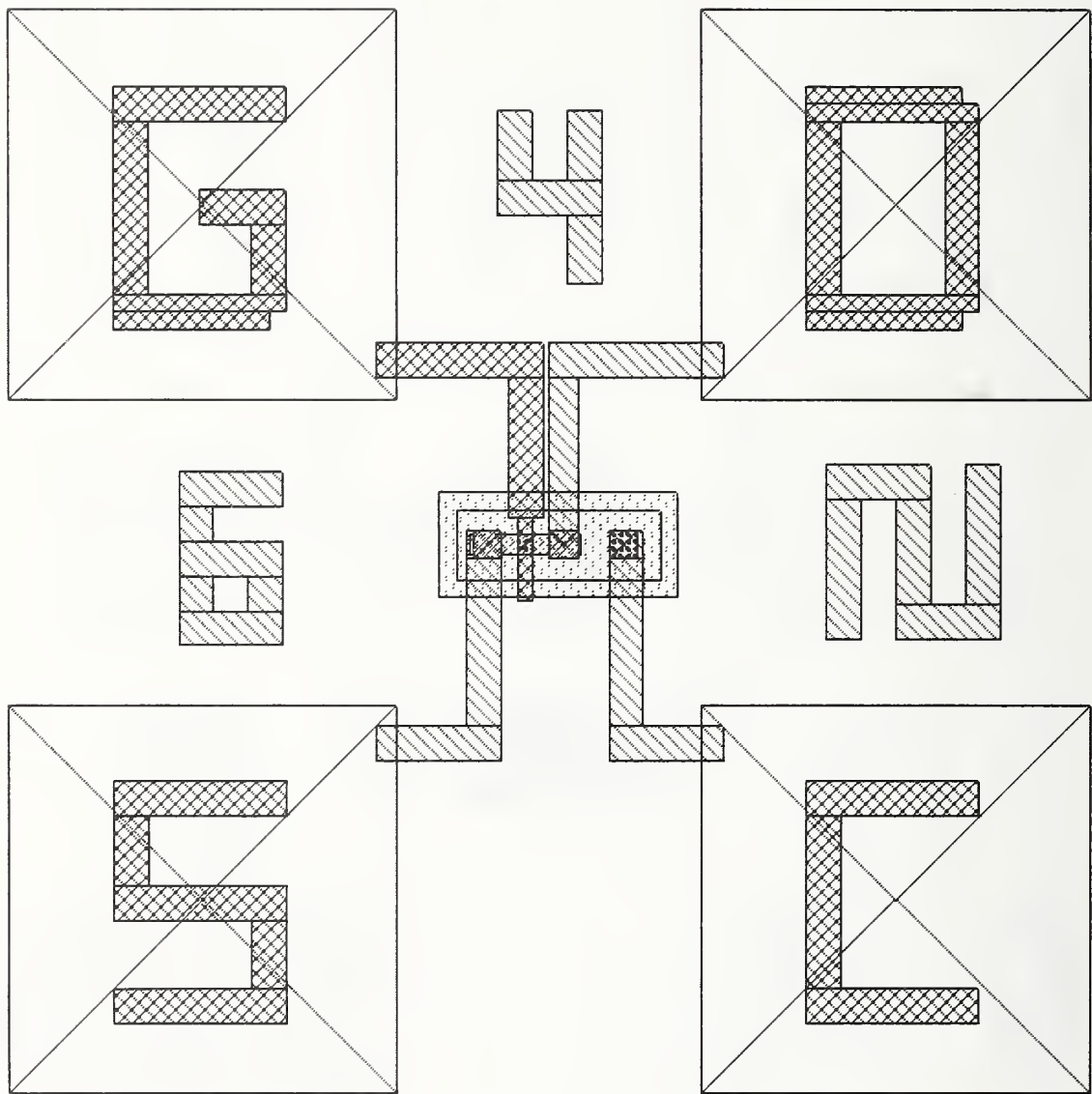


Figure 14. *N*-channel depletion-mode MOSFET found in the test library and NIST9.

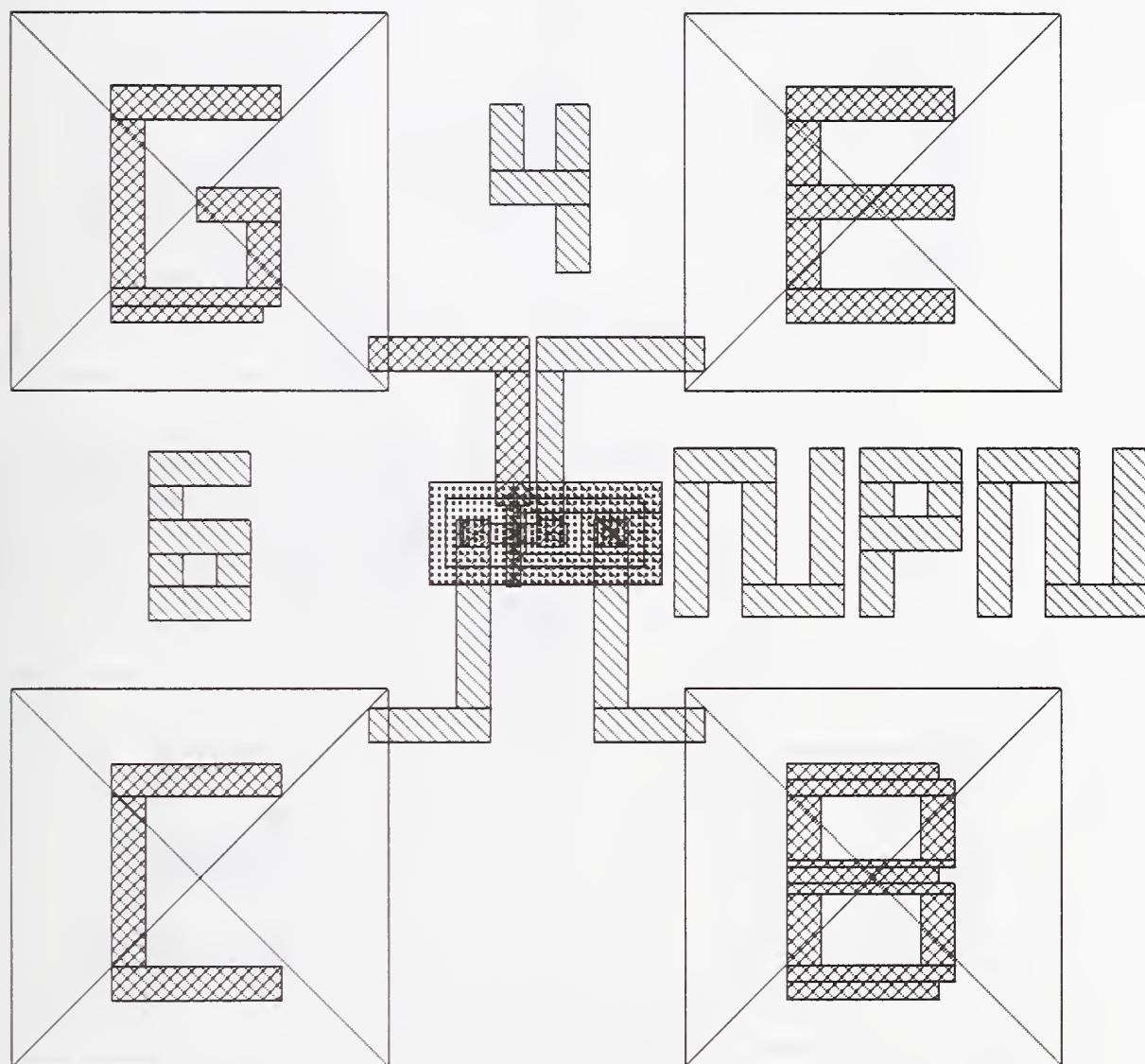


Figure 15. First bipolar design (*npn*) on NIST9 with the base contact beside the emitter and with a full implant.



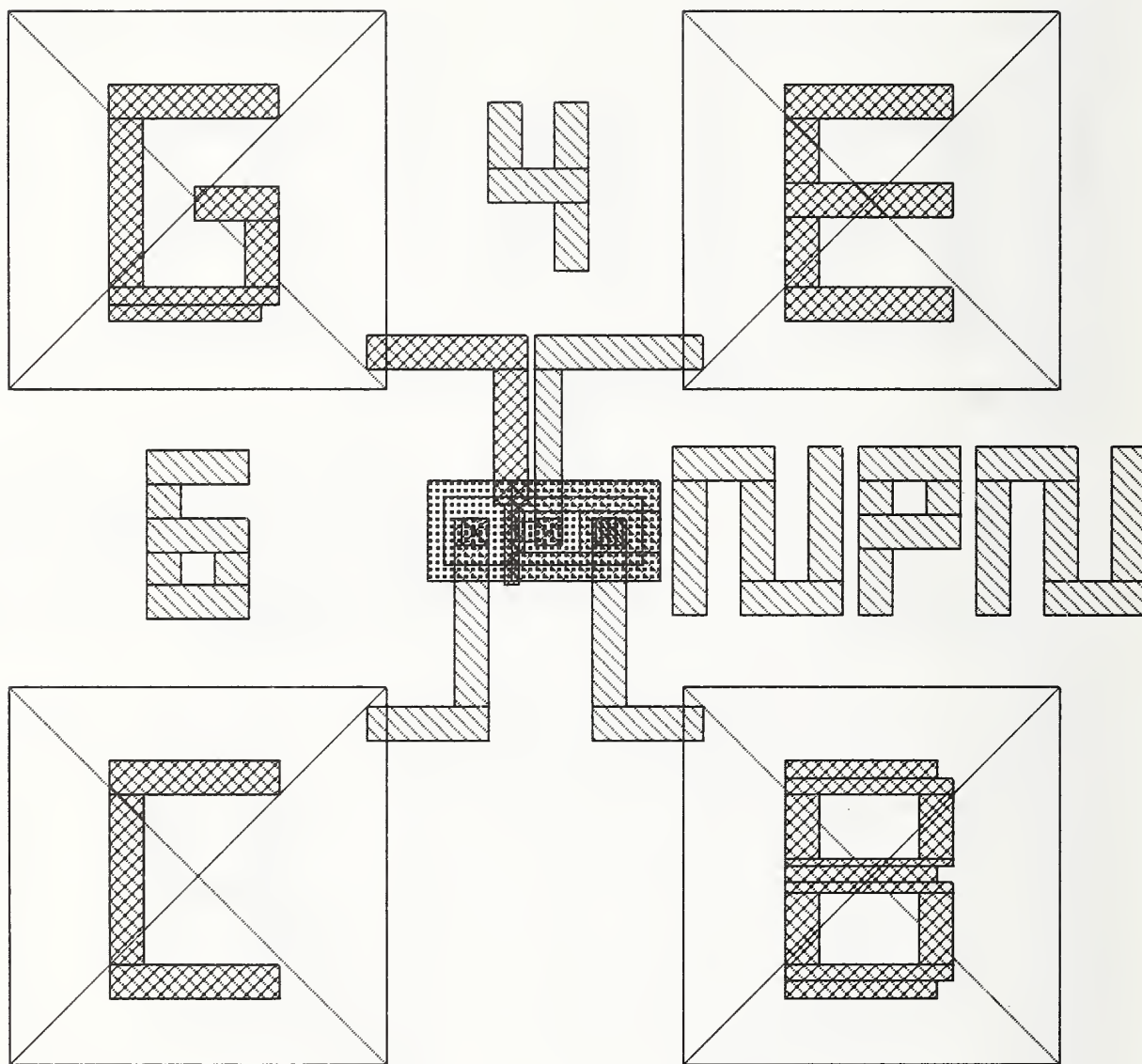


Figure 16. Second bipolar design (*npn*) on NIST9 with the base contact beside the emitter and with a half implant.

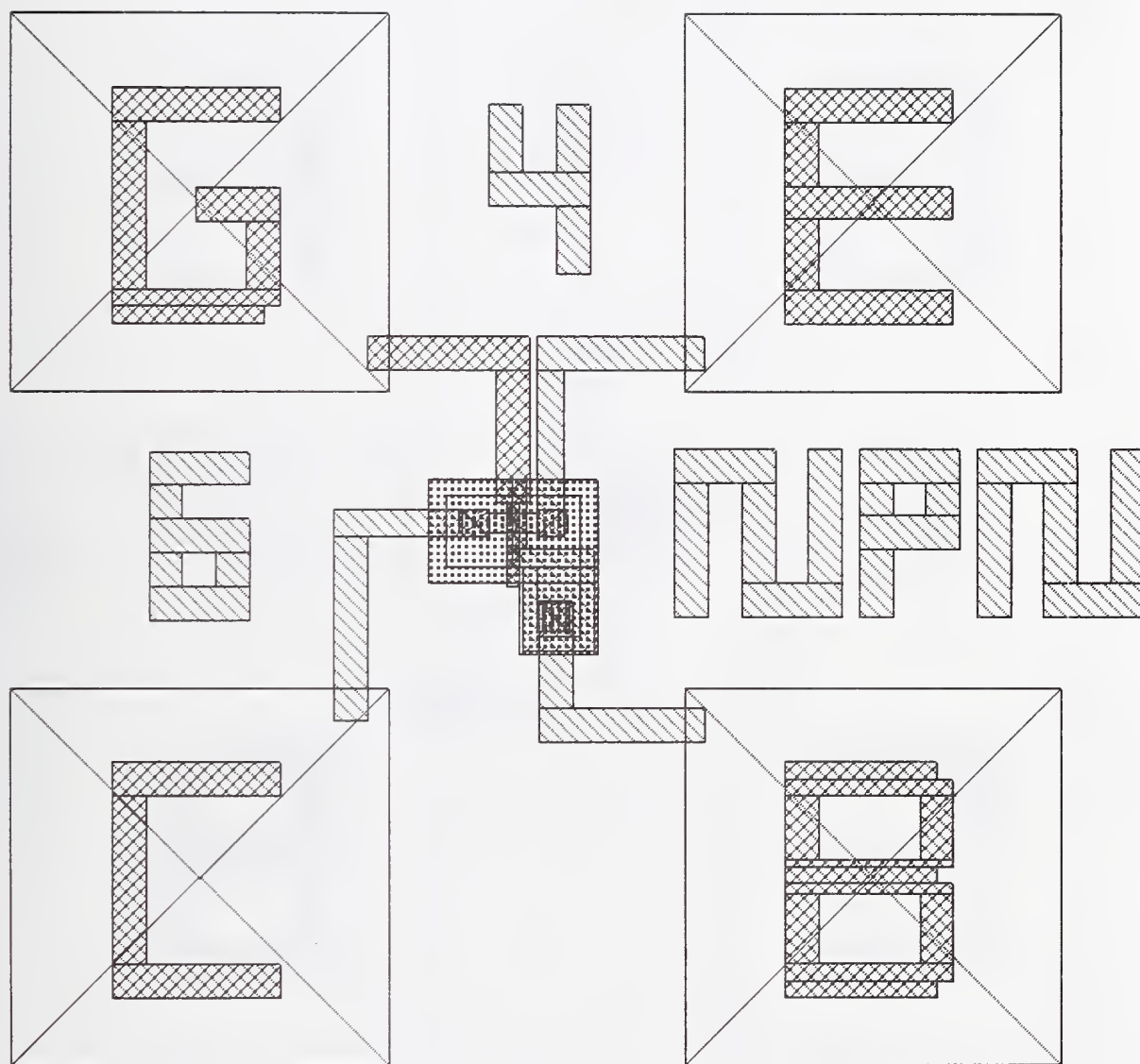


Figure 17. Third bipolar design (*npn*) on NIST9 with the base contact below the gate and with a full implant.

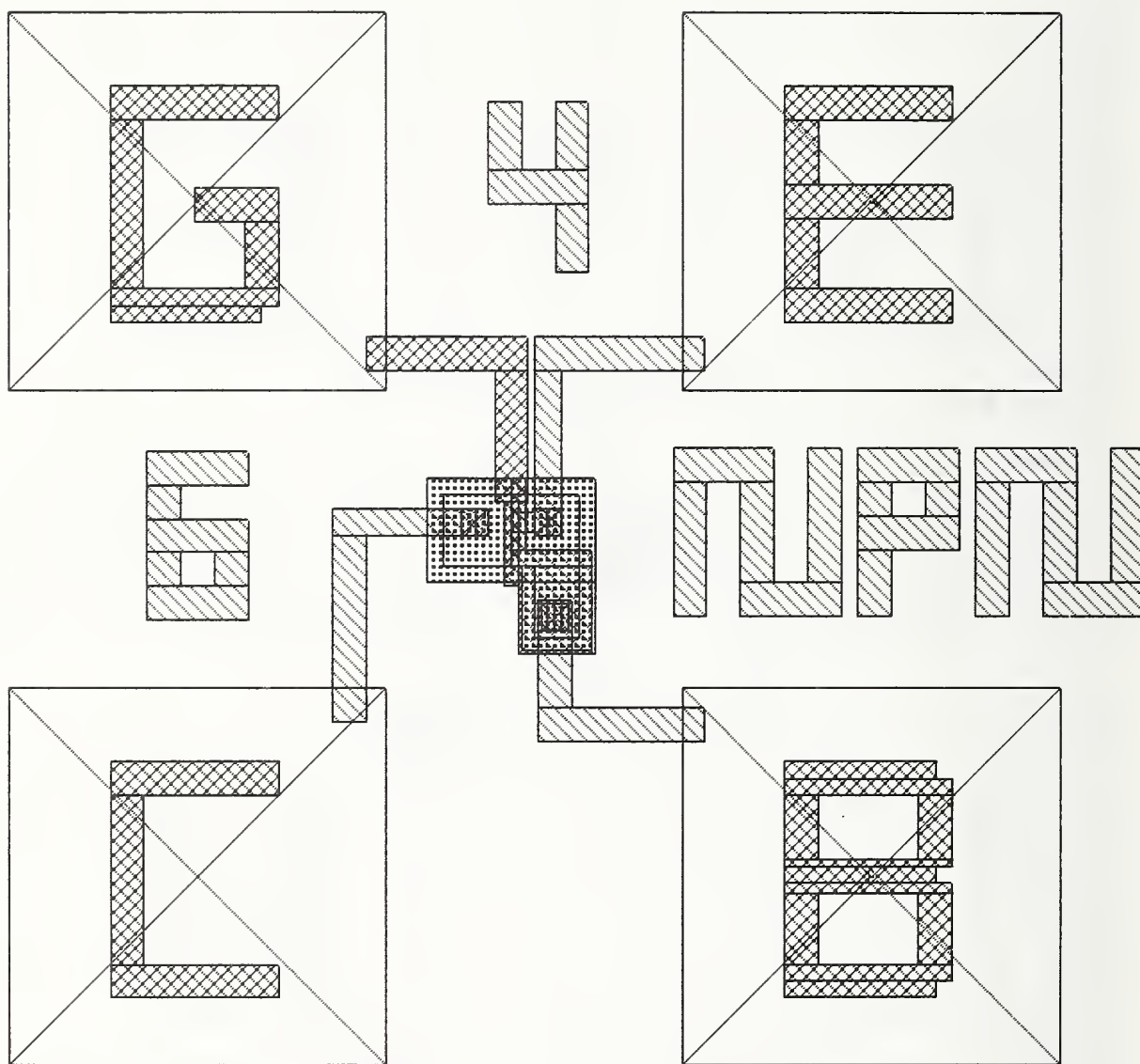


Figure 18. Fourth bipolar design (*npn*) on NIST9 with the base contact below the gate and with a half implant.



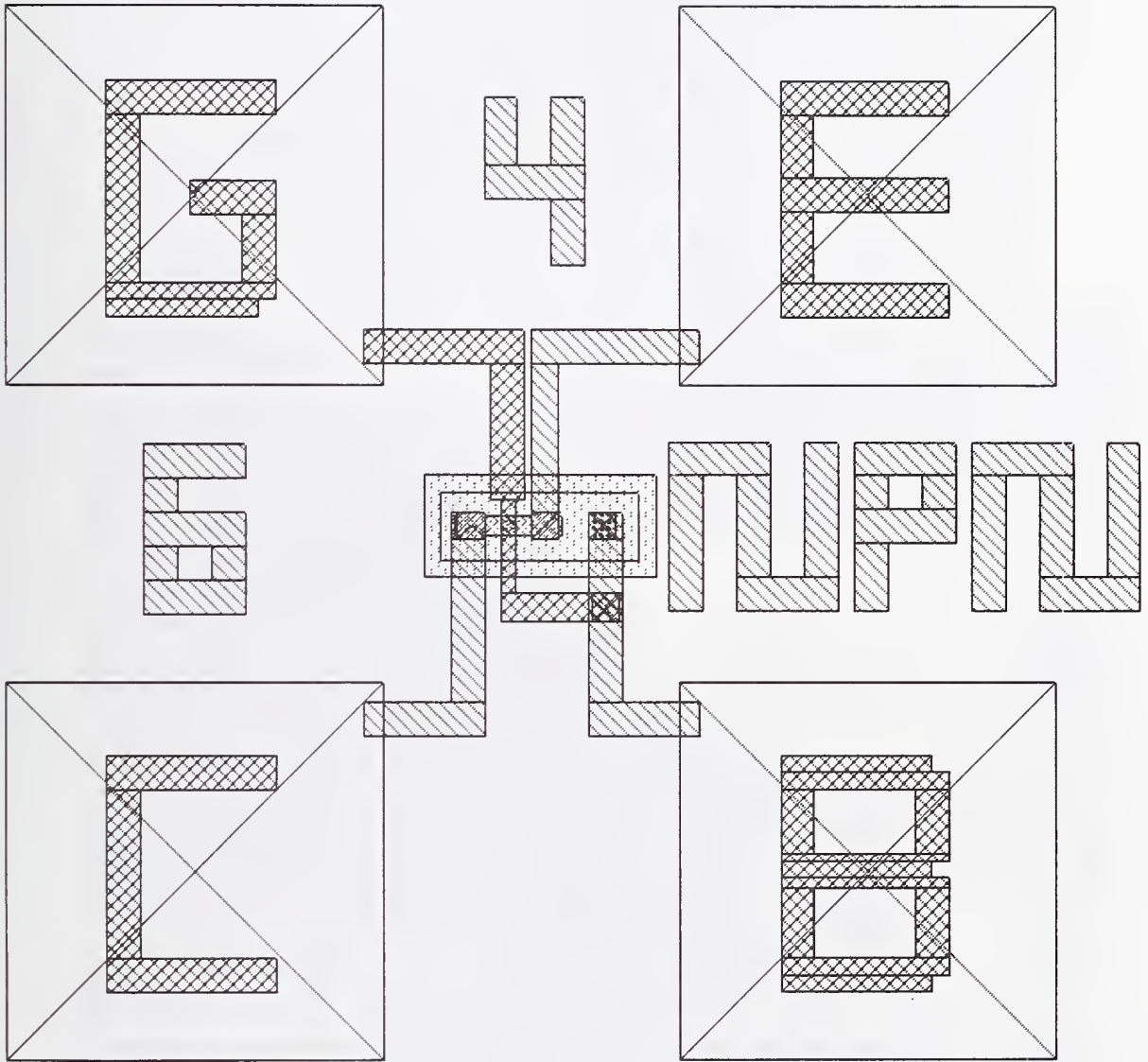


Figure 19. Fifth bipolar design (*npn*) on NIST9 with an *n*-channel MOSFET gate connected to its base.

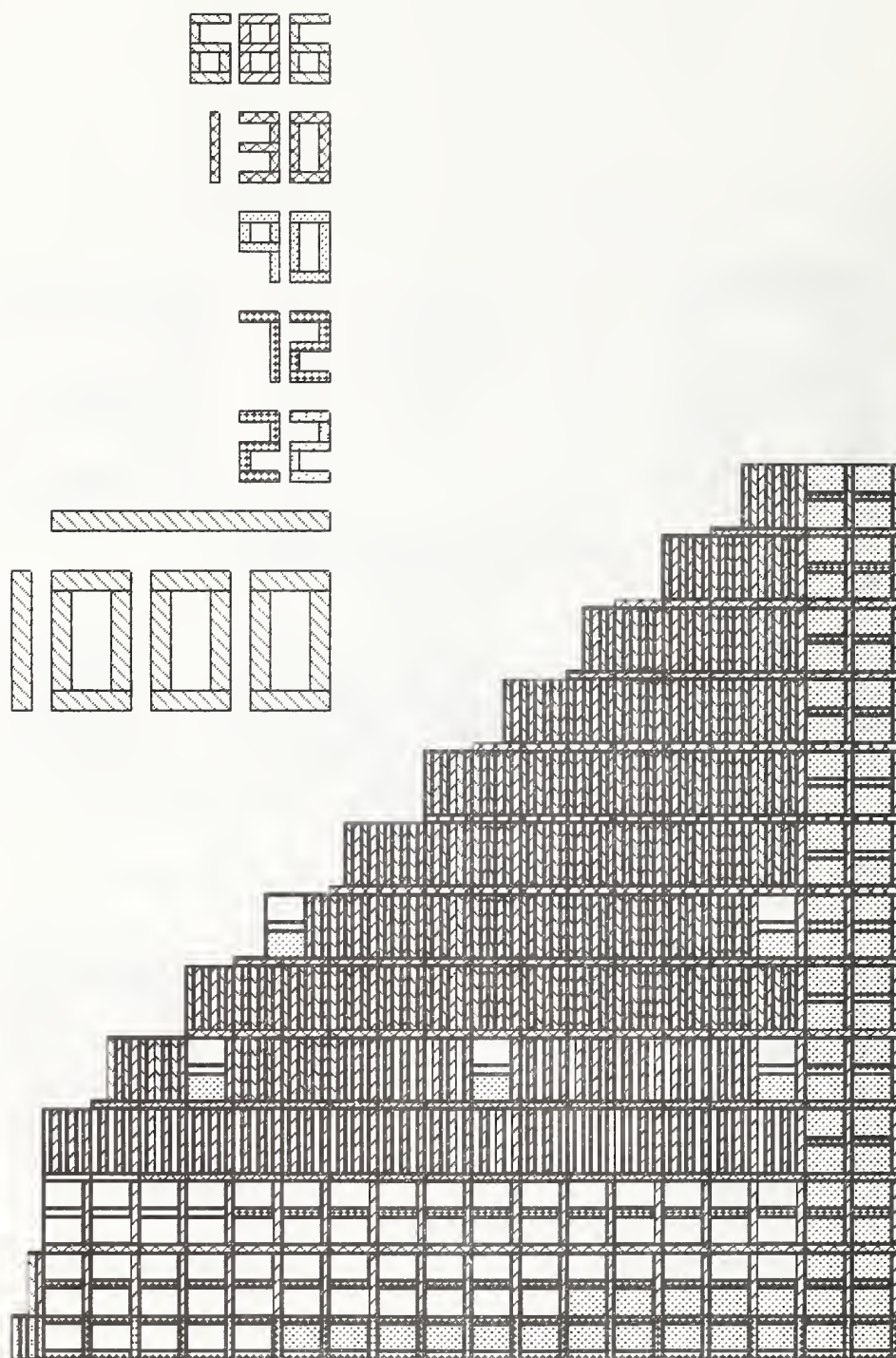


Figure 20. Cell structure of the test library with module count.



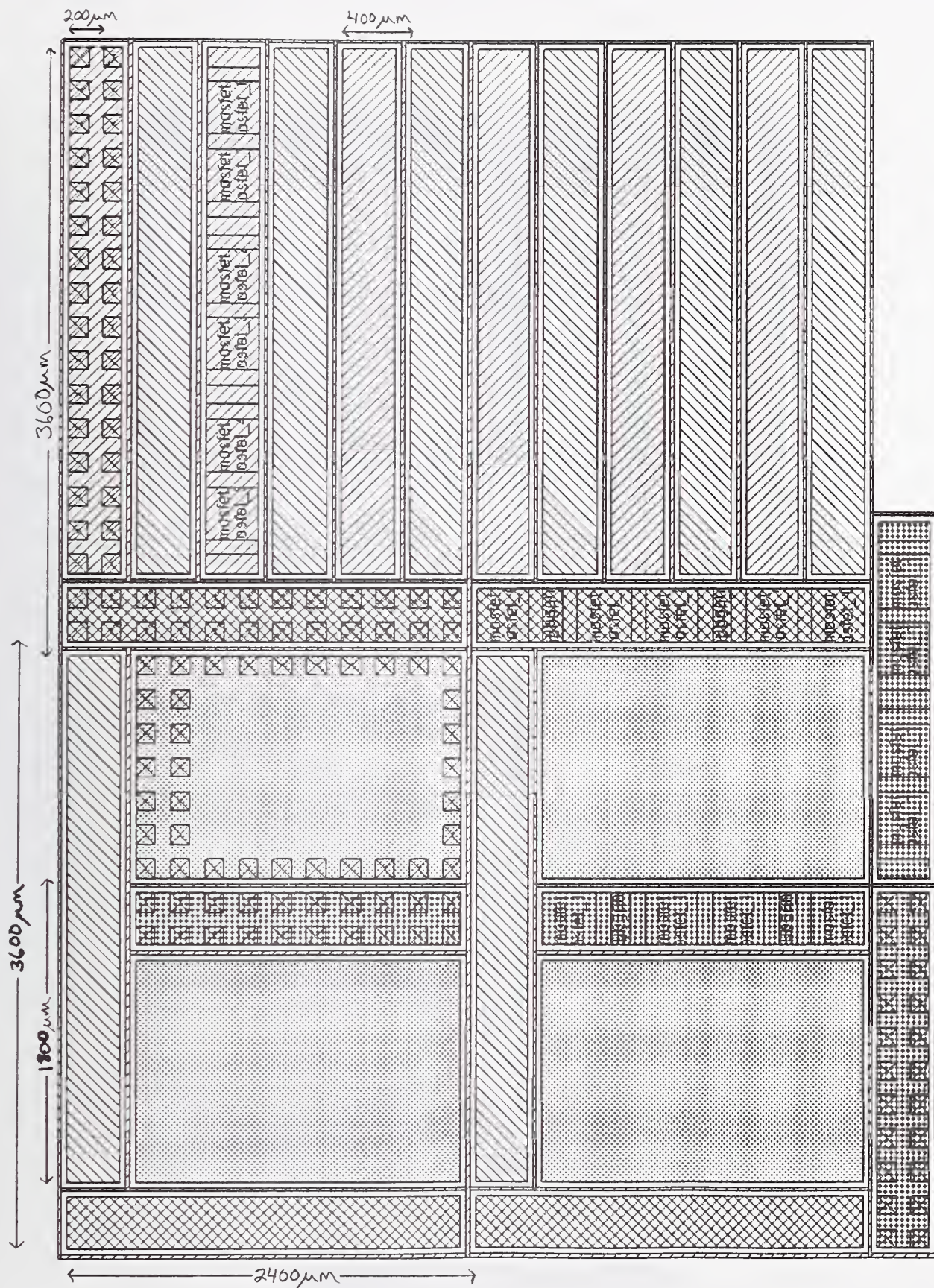


Figure 21. Module spacings used in the test library, NIST8, and NIST9.

AM	BM	CM	DM	KM	EM	UM	FM	VM	XM	AaM
AM_0	BM_0	CM_0	DM_0	KM_0	EM_0	UM_0	FM_0	VM_0	XM_0	AaM_0
aaM aaM_0						aaaM aaaM_0				
DDM DDM_0					BbM BbM_0	EEM EEM_0				
bbbM bbbM_0						cccM cccM_0				
GGM GGM_0						OOM OOM_0				

Figure 22. Cell structure of NIST8.





Figure 23. Subcell structure of NIST8.

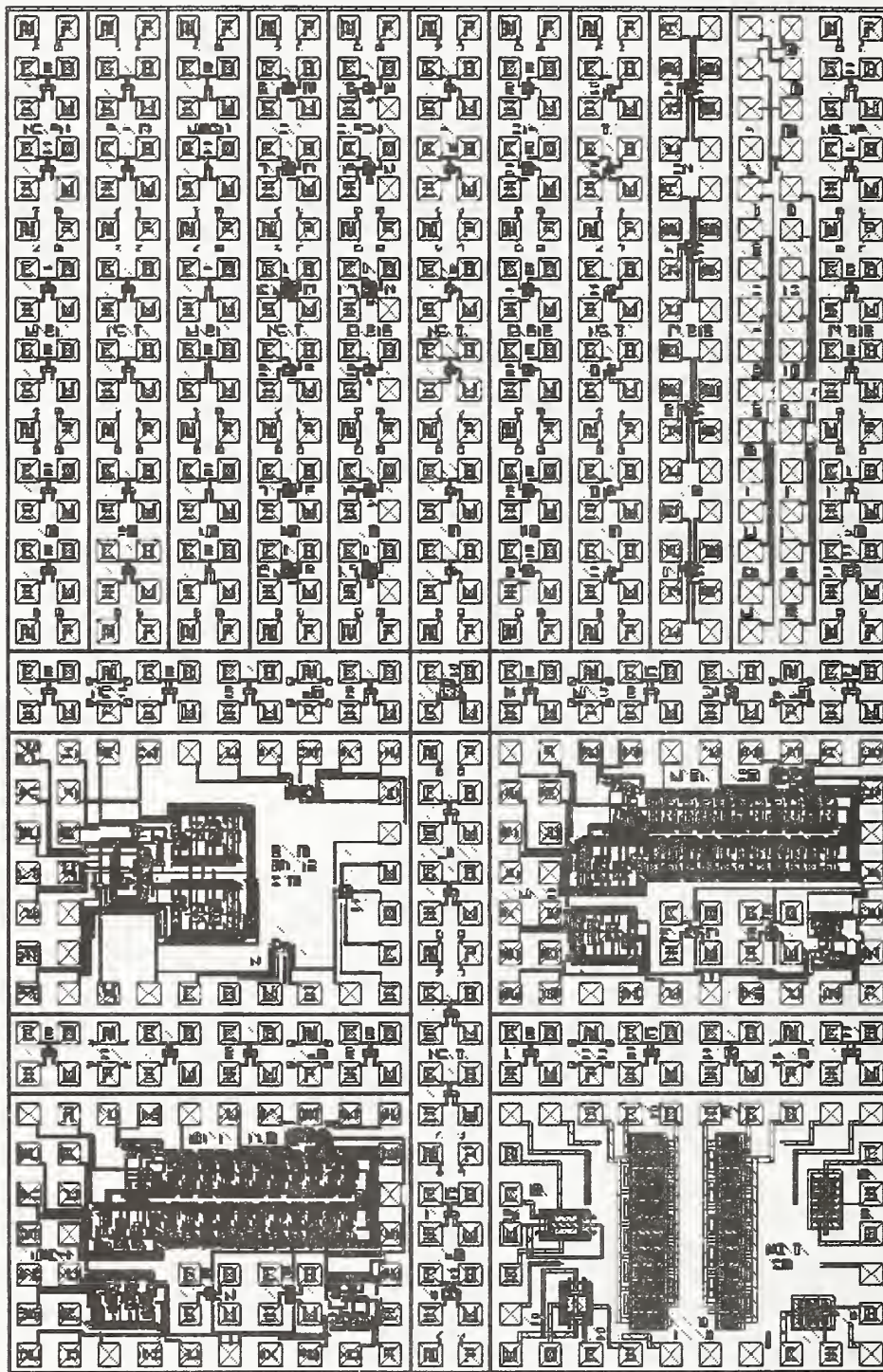


Figure 24. CMOS Test Chip, NIST8.



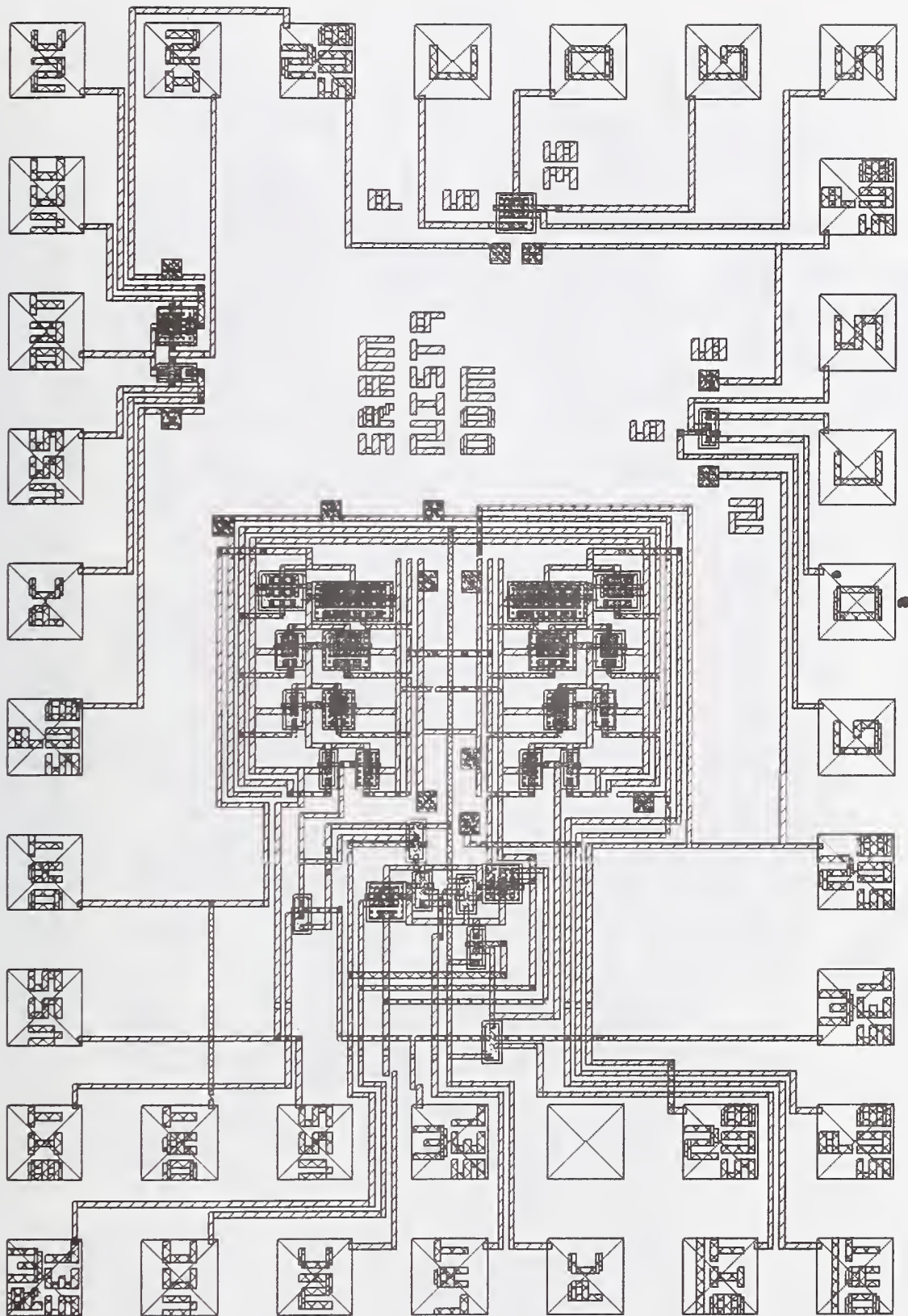


Figure 25. Static RAM module DDM found in the test library, NIST8, and NIST9.

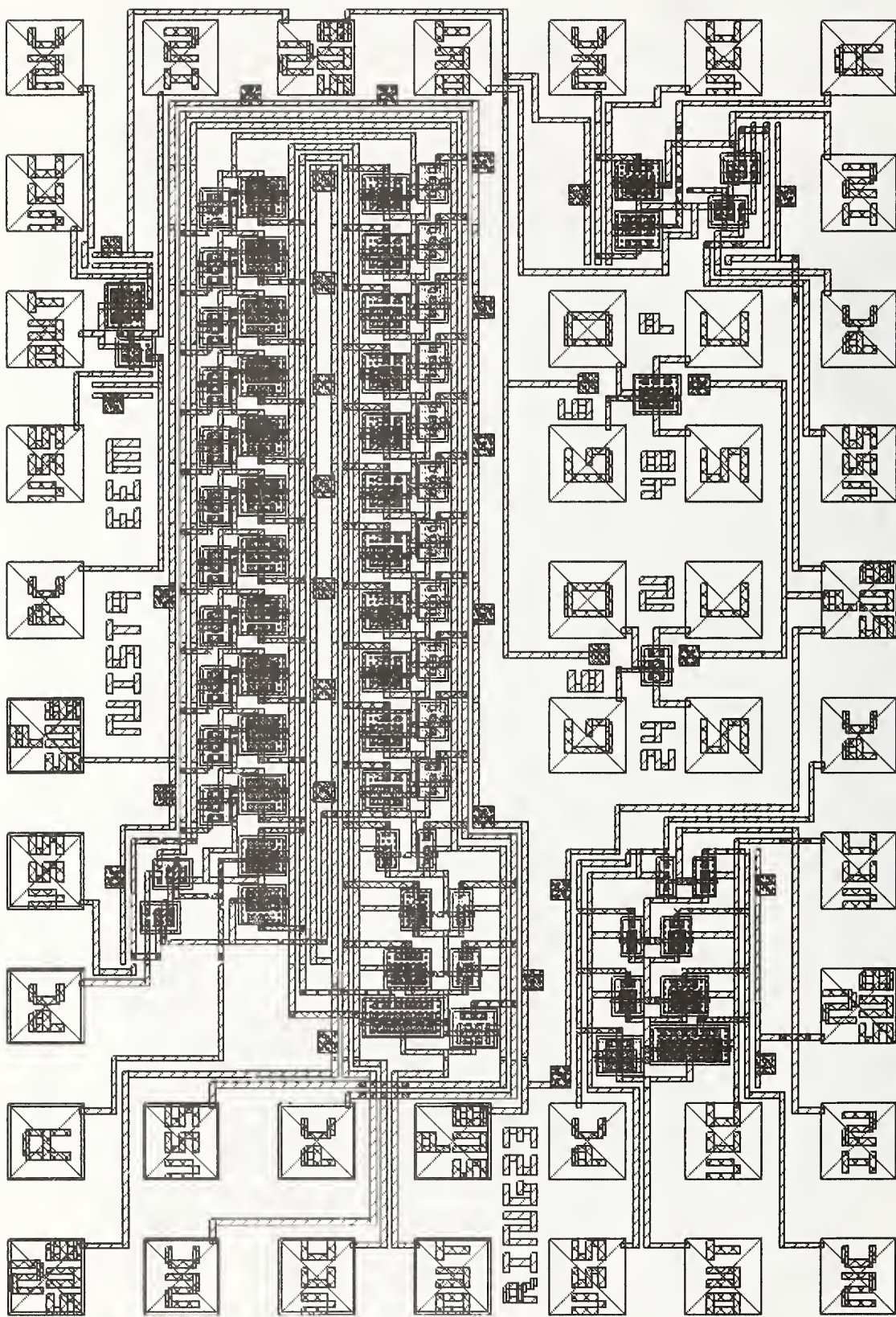


Figure 26. Ring oscillator module EEM found in the test library, NIST8, and NIST9.



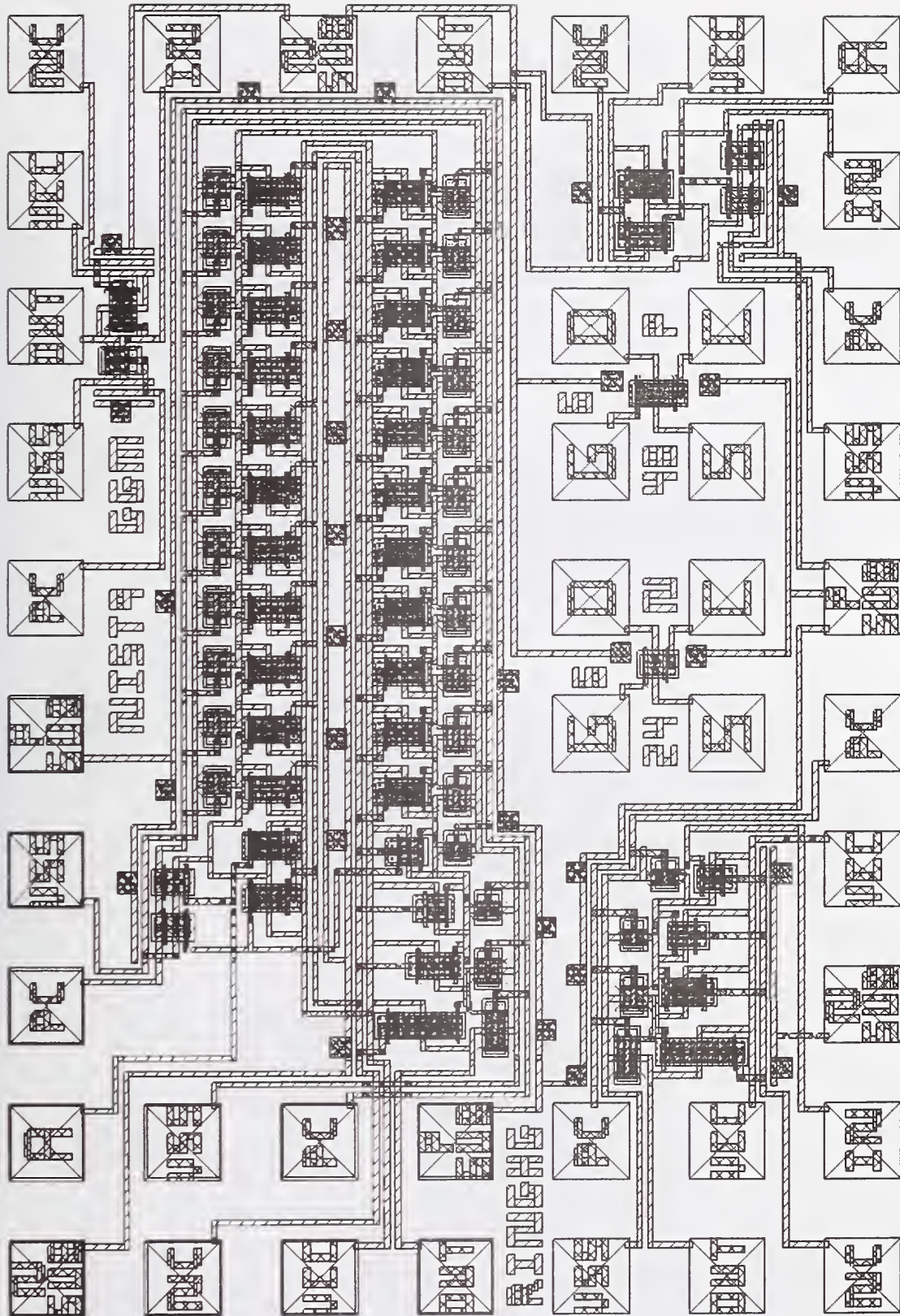


Figure 27. H-gate MOSFET ring oscillator module GGM found in the test library, NIST8, and NIST9.



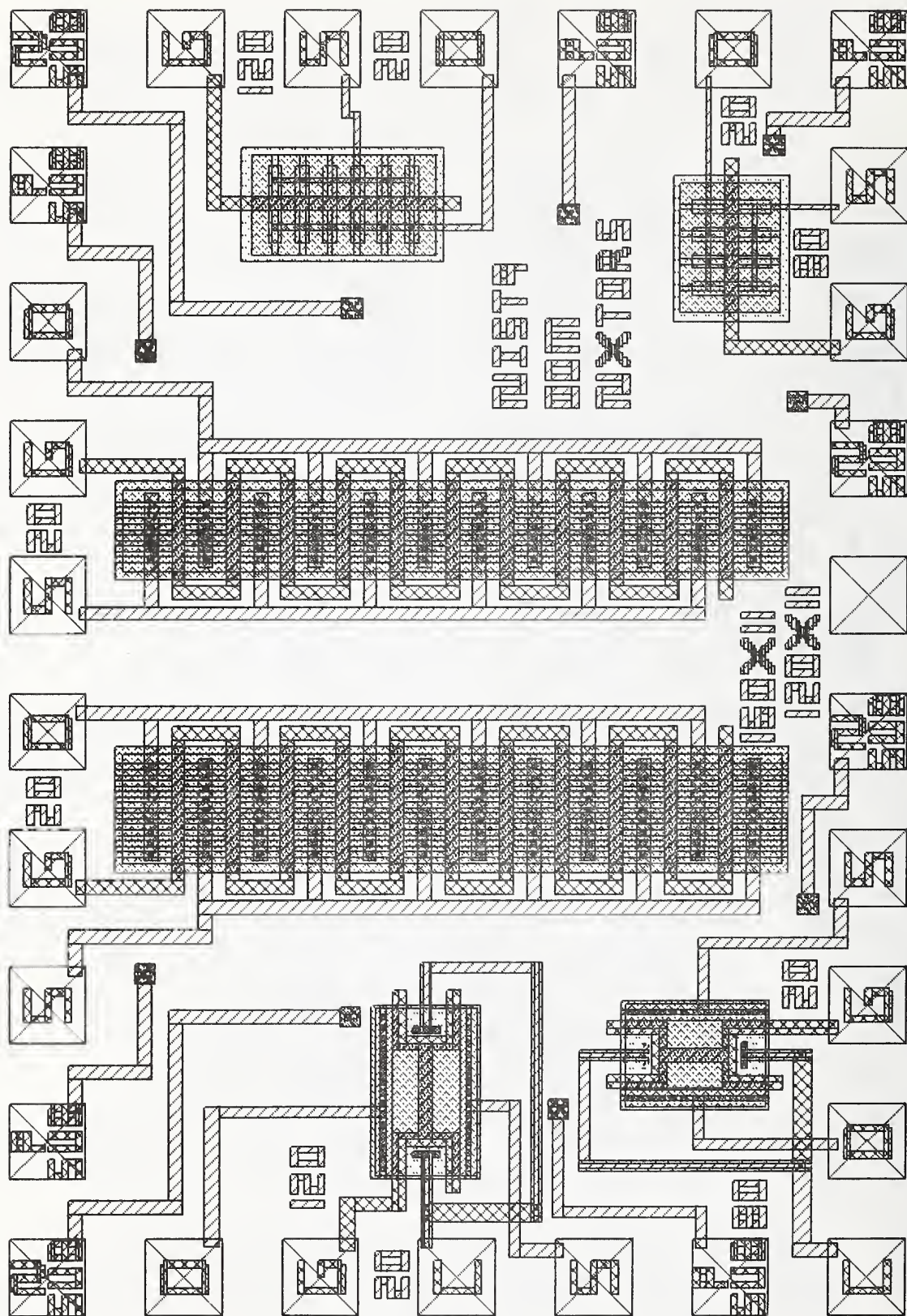


Figure 28. Large  $n$ -channel MOSFETs for radiation investigations (module OOM) found in the test library, NIST8, and NIST9.

UNSELECTED: LATCH = 0  
RWSEL = 0  
WSEL = 0

TO WRITE: LATCH = 1  
RWSEL = 1  
WSEL = 1

BIT = data to be written  
 $\overline{\text{BIT}}$  =  $\overline{\text{data to be written}}$

TO READ: RWSEL = 1  
WSEL = 0  
LATCH = 0

DATA = data in cell  
 $\overline{\text{DATA}}$  =  $\overline{\text{data in cell}}$

THEN: RWSEL = 0

THEN: LATCH = 0  
RWSEL = 0  
WSEL = 0

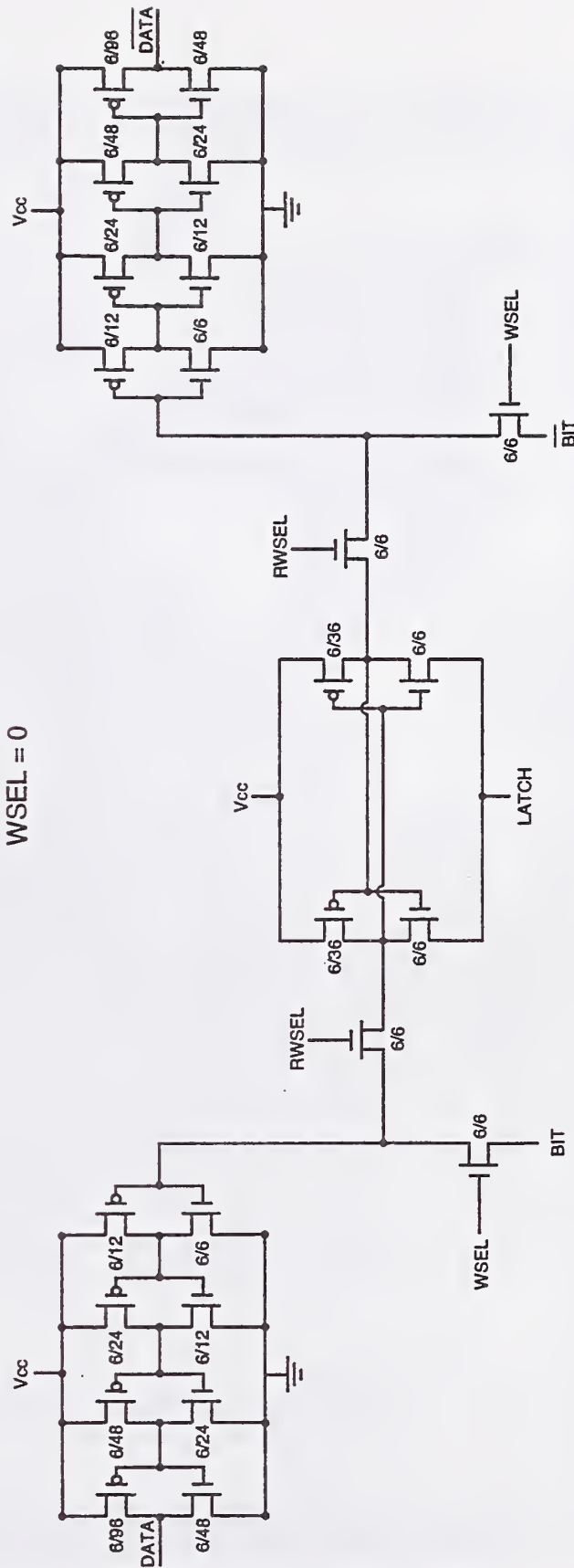


Figure 29. Circuit diagram of the static RAM cell (and how to test it).

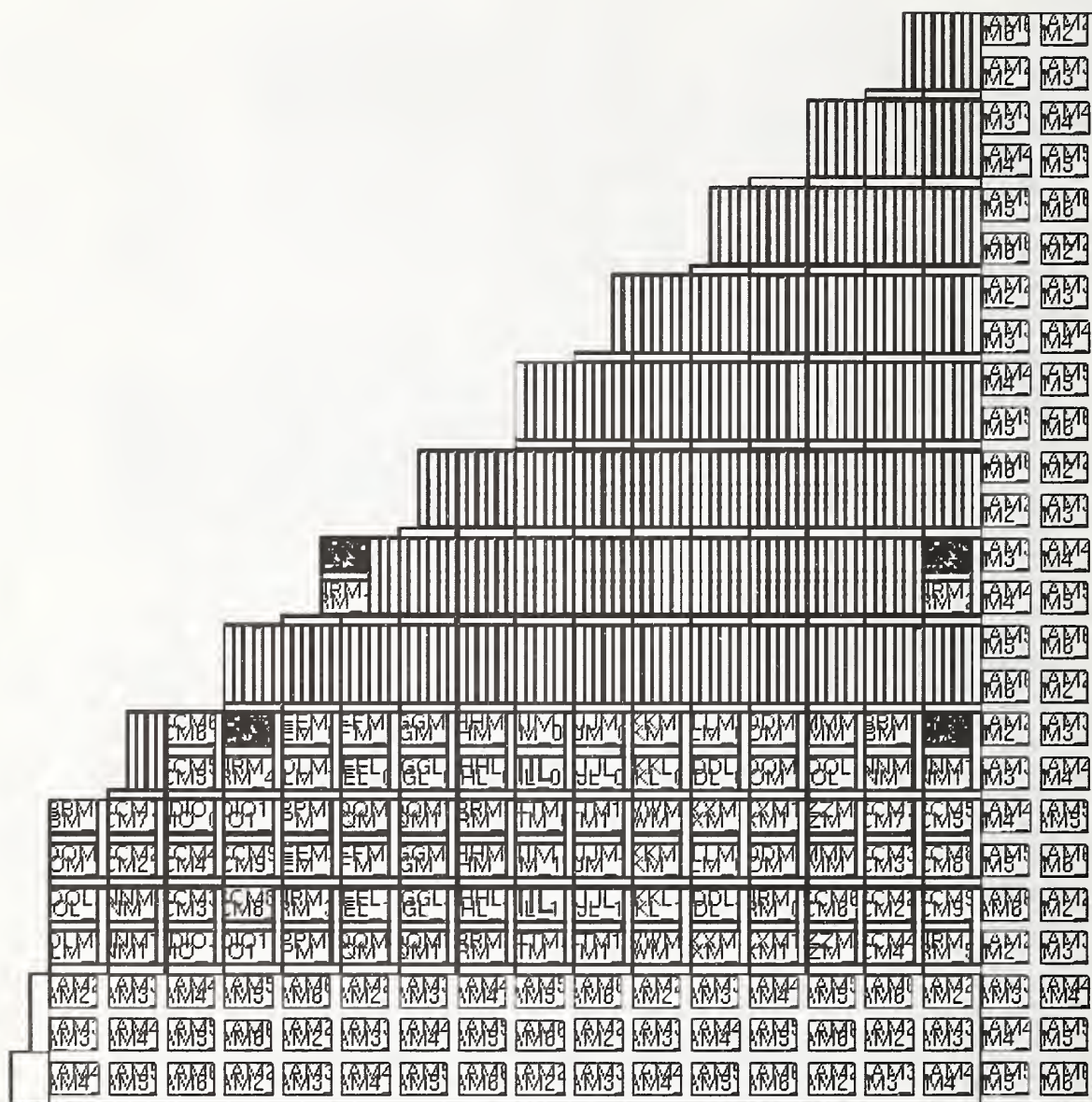


Figure 30. Cell structure of the SOI/SIMOX test wafer NIST9.





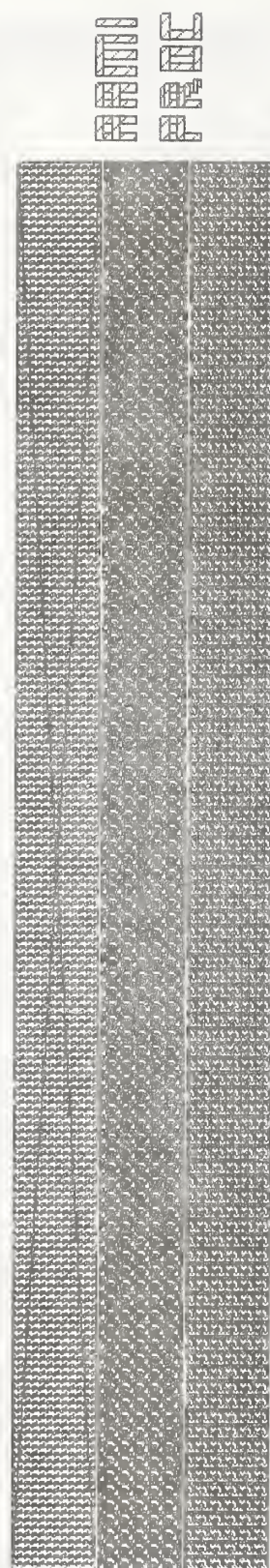


Figure 32. Processing module AAM1 found in the test library and NIST9.



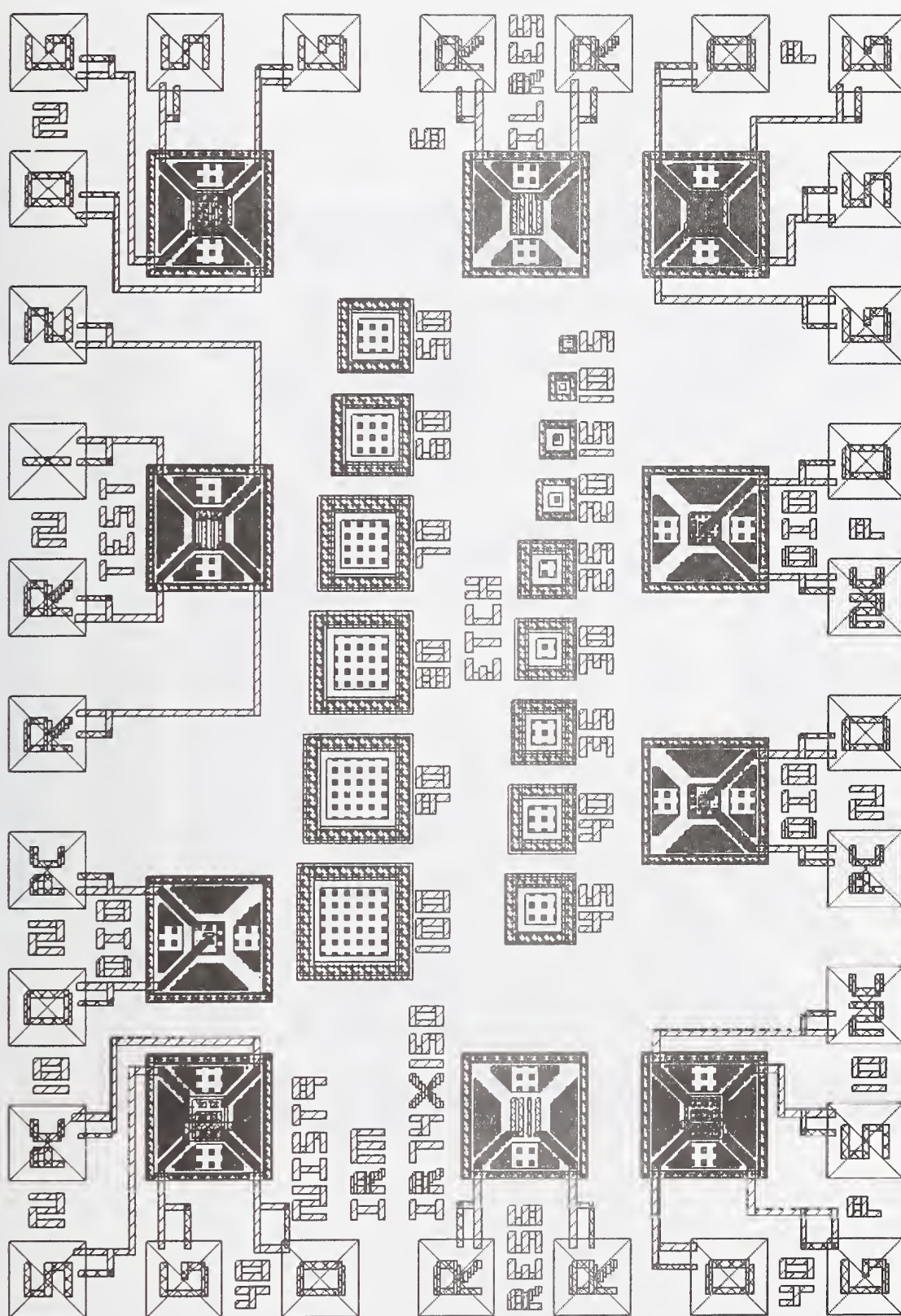


Figure 33. Micromachining module IRM found in the test library and NIST9.

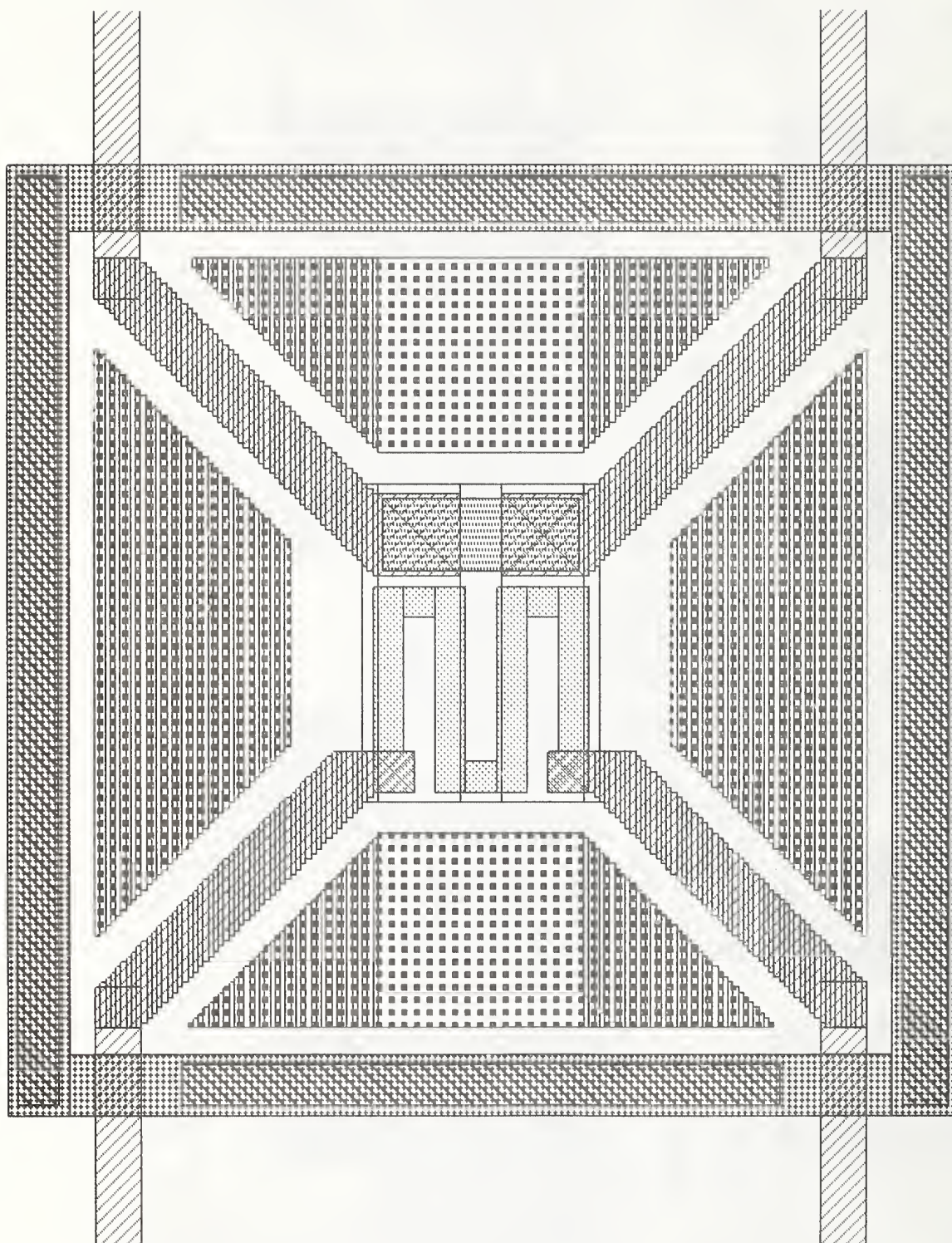


Figure 34. OH breath analyzer.



Table 1 - Doses and Energies for the Implantations on NIST9

IMPLANT MASK	DOPANT	DOSES AND ENERGIES (ASSUMING T=0.15 UM)
1. <i>N</i> well	Phosphorus	$8 \times 10^{11}/\text{cm}^2 @ 50 \text{ keV} = 5.33 \times 10^{16}/\text{cm}^3$
2. <i>P</i> well	Boron	$8 \times 10^{11}/\text{cm}^2 @ 20 \text{ keV} = 5.33 \times 10^{16}/\text{cm}^3$
3. <i>N</i> tie	Phosphorus	$3 \times 10^{13}/\text{cm}^2 @ 50 \text{ keV} = 2.0 \times 10^{18}/\text{cm}^3$
4. <i>P</i> tie	Boron	$3 \times 10^{13}/\text{cm}^2 @ 20 \text{ keV} = 2.0 \times 10^{18}/\text{cm}^3$
5. D-implant	Phosphorus	$2 \times 10^{12}/\text{cm}^2 @ 50 \text{ keV} = 1.33 \times 10^{17}/\text{cm}^3$
6. <i>N</i> -implant	Phosphorus	$3 \times 10^{15}/\text{cm}^2 @ 50 \text{ keV} = 2.0 \times 10^{20}/\text{cm}^3$
7. <i>P</i> -implant	Boron	$3 \times 10^{15}/\text{cm}^2 @ 20 \text{ keV} = 2.0 \times 10^{20}/\text{cm}^3$
IMPLANT MASK	DOPANT	DOSES AND ENERGIES (ASSUMING T=0.50 UM)
8. <i>N</i> poly	Phosphorus	$5 \times 10^{14}/\text{cm}^2 @ 180 \text{ keV} = 1.0 \times 10^{19}/\text{cm}^3$
9. <i>P</i> poly	Boron	$5 \times 10^{14}/\text{cm}^2 @ 60 \text{ keV} = 1.0 \times 10^{19}/\text{cm}^3$

Table 2 - Mask Processing Sequence for NIST9

	MASK	CIF NAME	CALMA NUMBER*	CLEAR (C) OR DARK (D) FIELD
1.	Island	SIL	1	C
2.	Nwell	SWN	2	D
3.	Pwell	SWP	3	D
4.	Ntie	SNT	4	D
5.	Ptie	SPT	5	D
6.	D-implant	SDF	6	D
7.	Npoly	SNP	7	D
8.	Ppoly	SPP	8	D
9.	Polysilicon	SPG	9	C
10.	N-implant	SND	10	D
11.	Subcon	SCS	11	D
12.	P-implant	SPD	12	D
13.	Contacts	SCT	13	D
14.	M1	SMF	14	C
15.	Glass	SOG	15	D
	(optional)			

Die Size:  $x = 44,820 \mu\text{m}$   $y = 45,020 \mu\text{m}$  (before and after CIF)

The smallest dimension for each mask was  $1 \mu\text{m}$  appearing in subcell chevron.mag.

\* Mask data can be presented to the mask maker using Calma numbers as well as CIF names.

Table 3 - Magic Layer Used for MOSFET Gates or a Shield for Bipolar Devices and the Mask Numbers Involved in the Processing

FET OR BIPOLAR STRUCTURE	MAGIC LAYER	MASKS USED
1. <i>n</i> -channel MOSFET gates (and surrounding poly)	poly	7 & 8 (poly & npoly)
2. <i>p</i> -channel MOSFET gates (and surrounding poly)	ppoly	7 & 9 (poly & ppoly)
3. most <i>npn</i> shields (and surrounding poly)	etch	7 & 8 (poly & npoly)
4. most <i>pnp</i> shields (and surrounding poly)	petch	7 & 9 (poly & ppoly)



Table 4 - Magic Layers, CIF Names, and Calma Numbers (as found in the Cifoutput Section of the Technology File) Associated with the SOI Masks

MASK DEFINITION	MAGIC LAYERS INCLUDED	SOI CIF NAME	CALMA NUMBER
1. allIsland, pad,ppad	il,ilc pad,ppad	SIL	1
2. allNwell	nw,nwc	SWN	2
3. allPwell	pw,pwc	SWP	3
4. ntie	ntie	SNT	4
5. ptie	ptie	SPT	5
6. dfet,grow 200 dimplant	dfet dimplant	SDF	6
7. pad,ppad shrink 200 allNpoly,allPpoly, etch,petch grow 100,shrink 100	pad,ppad poly,ppoly,pc,ppc nfet,dfet,pfet ndpc,pdpc etch,petch	SPG	7
8. pad,shrink 200 allNpoly,etch grow 100,shrink 100	pad poly,nfet,dfet pc,ndpc,etch	SNP	8
9. ppad,shrink 200 allPpoly,petch grow 100,shrink 100	ppad ppoly,pfet ppc,pdpc,petch	SPP	9
10. allNdiff	ndiff,ndc,nndiff,nwc nfet,dfet,ndpc	SND	10
11. substrate, subcon,open	substrate subcon,open	SCS	11
12. allPdiff	pdiff,pdc,ppdiff,pwc pfet,pdpc	SPD	12
13. subcon,pad,ppad shrink 800 contacts shrink 200 open,hole	subcon,pad,ppad ndc,pdc,nwc,pwc pc,ppc,ilc ndpc,pdpc open,hole	SCT	13
14. pad,ppad shrink 400 allMetal1 grow 200,shrink 200	pad,ppad m1,pc,ppc,ndpc,pdpc ndc,pdc,nwc,pwc ilc,subcon	SMF	14
15. pad,ppad shrink 600 glass,open	pad,ppad glass open	SOG	15

Table 5 - Magic Layers, CIF Names, and Calma Numbers (as found in the Cif-output Section of the Technology File) Associated with the MOSIS CMOS Masks

MASK DEFINITION	MAGIC LAYERS INCLUDED	CMOS CIF NAME	CALMA NUMBER
1. allNwell	nw,nwc	CWN	1
2. allPwell	pw,pwc	CWP	2
3. pad shrink 400 allMetal2	pad m2 m2c	CMS	3
4. pad shrink 200 allMetal1,m2c	pad,m1,pc,ppc ndpc,pdpc ndc,pdc nwc,pwc ilc,subcon m2c	CMF	4
5. allPoly pad	poly,ppoly,pc,ppc nfet,pfet,dfet ndpc,pdpc pad	CPG	5
6. allNdiff allPdiff and allIsland	ndiff,ndc nndiff,nwc nfet,dfet,ndpc pdiff,pdc ppdiff,pwc pfet,pdpc il,ilc	CAA	6
7. pad shrink 400 m2c shrink 100	pad m2c	CVA	7
8. ndiff,nfet grow 200 allNdiff	ndiff,nfet ndc,nndiff,dfet nwc,ndpc	CSN	8
9. pdiff,pfet grow 200 allPdiff	pdiff,pfet pdc,ppdiff pwc,pdpc	CSP	9
10. ndc,pdc,pwc,nwc shrink 200	ndc,pdc,pwc,nwc	CCA	10
11. pad shrink 100 pc,ndpc,pdpc shrink 200	pad pc,ndpc,pdpc	CCP	11
12. pad shrink 600 glass	pad glass	COG	12

Table 6 - Module Cell Names, Dimensions, and Pad Arrangement for the Different Module Sizes Followed by the MOSFET Dimensions and Sample Subcell Name for the 2 by 16 Small, Medium, and Large Modules

MODULE NAMES	DIMENSIONS	PAD ARRANGEMENT
1. AAS to ZZS AAM to ZZM AAL to ZZL DLM,IRM,DIO,DIO1	width = 1912 $\mu\text{m}$ height = 1312 $\mu\text{m}$	10 by 7 30 pads (10 top, 10 bottom 7 right, 7 left)
2. AS to ZS AM to ZM AL to ZL AaM to ZzM	width = 312 $\mu\text{m}$ height = 3112 $\mu\text{m}$	2 by 16
3. aaS to zzS aaM to zzM aaL to zzL	width = 2312 $\mu\text{m}$ height = 312 $\mu\text{m}$	12 by 2
4. aaaS to zzzS aaaM to zzzM aaaL to zzzL AAM1	width = 1912 $\mu\text{m}$ height = 312 $\mu\text{m}$	10 by 2
5. aaaaS to zzzzS aaaaM to zzzzM aaaaL to zzzzL	width = 312 $\mu\text{m}$ height = 2112 $\mu\text{m}$	2 by 11

MODULE SIZE	MOSFET CHANNEL DIMENSIONS	SAMPLE SUBCELL NAME
A. Small modules (ending with 'S')	L = 0.2, 0.3, 0.4, 0.5, 0.6, 0.8 $\mu\text{m}$ W = 6 $\mu\text{m}$	pl02w6
B. Medium modules (ending with 'M')	L = 2, 3, 4, 5, 6, 8 $\mu\text{m}$ W = 6 $\mu\text{m}$	nl2w6
C. Large modules (ending with 'L')	L = 12, 13, 14, 15, 16, 18 $\mu\text{m}$ W = 6 $\mu\text{m}$	nl12w6min



Table 7 - Method Used to Make a Medium Module into a Small Module on NIST9

---

---

```
% cd~/simox
% cp BM.mag B.mag
% magic B
    change label to BS
    delete the cells
    rename the cells for the appropriate dimensions
    replace the cells in the module
    change labeled dimensions
    :cif ostyle asis
    :cif
    :writeall
    :quit
% cd~/simoxsub
% cp~/simox/B.cif
% magic -Tsimox junk
    :cif istyle in10x
    :cif read B
    :writeall
    :quit
% cp B.mag B100.mag
% rm B.mag
% magic B100
    use the appropriate subcon cells (e.g., subconupS and subconS)
    edit the cells for the correct submicron dimensions
    :writeall
    :quit
% cp B100.mag BS.mag
% magic waferS
    :getcell BS
    :writeall
    :quit
```

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Table 8 - Module Name, Label, and Description for the Large 10 by 7 Modules

MODULE S M L			MODULE LABEL	DESCRIPTION
-	AAM	-	PROC	Processing structures
-	AAM2	-	PROC-RES	Processing structures Two resistors with $L=500\text{ }\mu\text{m}$ , $W=1500\text{ }\mu\text{m}$ 1. $n_{\text{well}}$ = channel $n_{\text{diff}}$ = source/drain 2. $p_{\text{well}}$ = channel $p_{\text{diff}}$ = source/drain
-	AAM3	-	PROC-TRAN	Processing structures Two transistors with $L=500\text{ }\mu\text{m}$ , $W=1500\text{ }\mu\text{m}$ 1. $n$ -channel MOSFET 2. $p$ -channel MOSFET
-	AAM4	-	PROC-ITRAN	Processing structures Two interdigitated MOSFETs ( $7\text{-}1500\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ gates) 1. $n$ -channel MOSFET 2. $p$ -channel MOSFET Two MOSFETs to probe during processing 1. $n$ -channel MOSFET, $L=10\text{ }\mu\text{m}$ , $W=20\text{ }\mu\text{m}$ 2. $p$ -channel MOSFET, $L=10\text{ }\mu\text{m}$ , $W=20\text{ }\mu\text{m}$
-	AAM5	-	PROC-SIMS	Processing structures - 6 SIMS targets ( $500\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$ ) for: $n_{\text{well}}$ , $n_{\text{tie}}$ , $n_{\text{diff}}$ $p_{\text{well}}$ , $p_{\text{tie}}$ , and $p_{\text{diff}}$
-	AAM6	-	PROC-SIMS	Processing structures - 6 SIMS targets ( $500\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$ ) for: $i_1$ , $\text{poly}$ , $m_1$ $\text{dimplant}$ , $p_{\text{poly}}$ , and $m_2$
-	BBM	-	NXTORS	Circular MOSFETs, multi-edged MOSFETs, many-fingered MOSFETs, and regular MOSFETs with same channel length - except for the one in the middle - gate = box $17 \times 17\text{ }\mu\text{m}$ with 7 reps - source/drain = box $20 \times 20\text{ }\mu\text{m}$ with 10 reps - $L=20\text{ }\mu\text{m}$ $W=2\pi(30)=188.4\text{ }\mu\text{m}$ - $L_{\text{mid}}=500\text{ }\mu\text{m}$ $W_{\text{mid}}=50\text{ }\mu\text{m}$
-	CCM	-	CAPS *	Capacitors with and without body contact ( $200 \times 200\text{ }\mu\text{m}$ )
-	CCM1	-	CAPS *	Miscellaneous capacitors ( $200 \times 200\text{ }\mu\text{m}$ )
-	CCM2	-	CAPS	Capacitor ( $1312 \times 1530\text{ }\mu\text{m}$ )

- CCM3 -	CAPS	Capacitors (1300 x 775 $\mu\text{m}$ )
		- m1/sub 22 pF with tox=8000 Å
		- m1/il 22 pF with tox=4000 Å
		- m1/poly 18 pF with tox=5000 Å
- CCM4 -	CAPS	Capacitors (1300 x 775 $\mu\text{m}$ )
		- poly/sub 22 pF with tox=4000 Å
		- il/sub 22 pF with tox=4000 Å
- CCM5 -	CAPS	Capacitors (1300 x 775 $\mu\text{m}$ )
		- ppoly/sub 22 pF with tox=4000 Å
		- m1/ppoly 18 pF with tox=5000 Å
- CCM6 -	CAPS	Capacitors (625 x 775 $\mu\text{m}$ )
		- poly/il 86 pF with tox=500 Å
		- ppoly/il 86 pF with tox=500 Å
		- ppoly/nndiff tox=500 Å
		- ppoly/ppdiff tox=500 Å
- CCM7 -	CAPS	Capacitors (1312 x 1530 $\mu\text{m}$ )
		- m1/poly/il/sub
- CCM8 -	CAPS	Capacitors (1312 x 1530 $\mu\text{m}$ )
		- m1/ppoly/il/sub
- CCM9 -	CAPS	Capacitors (625 x 775 $\mu\text{m}$ )
		- poly/il 86 pF with tox=500 Å
		- ppoly/il 86 pF with tox=500 Å
		- poly/nndiff tox=500 Å
		- poly/ppdiff tox=500 Å
DDS DDM DDL	SRAM	1-bit static RAM
		- with selected SRAM parts pinned out
EES EEM EEL	RING23	23-stage ring oscillator
		- ringinv (period=88), amp, nand
		nringinv
		pringinv
		$W_n/L_n = 24/6$
		$W_p/L_p = 48/6$
- FFM -	CIRC23	Ring oscillator with circular MOSFETs
		- ampcirc
		- ngate box 5x5 $\mu\text{m}$ with 3 reps L=6 $\mu\text{m}$
		- nS/D box 8x8 $\mu\text{m}$ with 5 reps
		$W_n=2\pi(13)=81.7 \mu\text{m}$
		$W_p=164 \mu\text{m}$
GGS GGM GGL	RINGHG	Ring oscillator with H-gate MOSFETs
HHS HHM HHL	RINGTG	Ring oscillator with T-gate MOSFETs
IIS IIM IIL	TIE23	Ring oscillator with MOSFETs using
		source-to-channel ties
		(period=56) - nl2w6tie
		ringtie



JJS JJM JJJ	HGTIE		Ring oscillator with H-gate MOSFETs using source-to-channel ties
KKS KKM KKL	TGTIE		Ring oscillator with T-gate MOSFETs using source-to-channel ties
- LLM -	CIRCNOC		Ring oscillator with circular MOSFETs with NO channel contact ampcirqnoc
- MMM -	SRAMCIRC		1-bit static RAM using circular MOSFETs - with selected SRAM parts pinned out sramcellcirq ampcirq $W_n=82 \mu\text{m}$ $W_p=6 \times W_n=492 \mu\text{m}$
- NNM -	VANPAUW		Van der Pauw structures $L_{mid} = 500 \mu\text{m}$ $W_{mid} = 50 \mu\text{m}$
- NNM1 -	VANPAUW		Van der Pauw structures (using ppoly plate) $L_{mid} = 500 \mu\text{m}$ $W_{mid} = 50 \mu\text{m}$
OOS OOM OOL	NXTORS		Multi-edge MOSFETs, multi-fingered MOSFETs, and italic H-gate MOSFETs
- PPM -	IL		Island meander structure - checks shorts, opens edges, straight horiz, vert make Kelvin measurement too
- QQM -	POL		Poly meander structure
- QQM1 -	PPOL		Ppoly meander structure
- RRM -	M1		M1 meander structure
- SSM -	M2	*	M2 meander structure
- TTM -	POLIL		Poly/island step coverage meander structure - checks poly/island step coverage - detects poly/island shorts - checks continuity - horiz, vert
- TTM1 -	PPOLIL		Ppoly/island step coverage meander structure
- UUM -	M2IL	*	M2/island step coverage meander structure
- VVM -	M2POL	*	M2/poly step coverage meander structure
- WWM -	M1IL		M1/island contact meander structure - tests step coverage - integrity of glass between m1 and island - detects m1/island shorts - checks continuity - horiz, vert
- XXM -	M1POL		M1/poly contact meander structure

-	XXM1	-	M1PPOL		M1/ppoly contact meander structure
-	YYM	-	M2M1	*	M2/m1 contact meander structure
-	ZZM	-	SUB		Substrate contact meander structure
					- tests continuity of m1 into subcon
					- horiz, vert
-	DLM	-	THREADDIS		Threading dislocation structures
-	IRM	-	IR74X150		Suspended structures
-	DIO	-	NDIODE		A meandering ndiode
					- for lifetime measurements
-	DIO1	-	PDIODE		A meandering pdiode
					- for lifetime measurements

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\* This module appears in the test library but not on NIST9.  
 Also, no small modules appear on NIST9.

FOR THE LARGE 10 BY 7 MODULES:

S (Small)	L=2 $\mu\text{m}$	$W_n=24 \mu\text{m}$
M (Medium)	L=6 $\mu\text{m}$	$W_p=48 \mu\text{m}$
L (Large)	L=10 $\mu\text{m}$	

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Table 9 - Module Name, Label, and Description for the 2 by 16 Modules, the 12 by 2 Modules, the 10 by 2 Modules, and the 2 by 11 Module

MODULE S M L	MODULE LABEL	DESCRIPTION
1. The 2 by 16 Modules-----		
AS AM AL	NCHAN	N-channel MOSFETs - nl2w6 - contacts 8x8
BS BM BL	PCHAN	P-channel MOSFETs - pl2w6 - contacts 8x8
CS CM CL	NMIN	Minimum sized MOSFETs - nl2w6min - contacts 8x8
- DM -	CIRC	Circular MOSFETs - nl6w82circ - contacts 8x8
ES EM EL	HG	H-gate MOSFETs - nl2w20hg - contacts 8x8
FS FM FL	TG	T-gate MOSFETs - nl2w20tg - contacts 8x8
- GM GL	TIE	MOSFETs with source-to-channel tie - nl2w20tie - contacts 8x8
HS HM HL	DFET	Depletion-mode MOSFETs - dl2w6 - contacts 8x8
IS IM IL	HGTIE	H-gate MOSFETs with source-to-channel tie - nl2w20hgtie - contacts 8x8
JS JM JL	TGTIE	T-gate MOSFETs with source-to-channel tie - nl2w20tgtie - contacts 8x8
- KM -	CIRCNOC	Circular MOSFETs with no channel contact - nl6w82circnoc - contacts 8x8
- LM -	CONRES	Contact resistors - conpoly4x4, conndiff4x4, conpdiff4x4, conil4x4



- MM -	CONRES		Contact resistors
			- conpoly6x6, conndiff6x6, conpdiff6x6, conil6x6
- NM -	CONRES		Contact resistors
			- conpoly8x8, conndiff8x8, conpdiff8x8, conil8x8
- OM -	CONRES		Contact resistors
			- conpoly16x16, conndiff16x16, conpdiff16x16, conil16x16
- PM -	CONRES	*	Contact resistors
			- convia4x4, conisl4x4, connw4x4, conpw4x4, convia4x4, conisl4x4
- PM1 -	CONRES		Contact resistors
			- conppoly4x4, conisl4x4, connw4x4, conpw4x4, conppoly4x4, conisl4x4
- QM -	CONRES	*	Contact resistors
			- constringvia, constringpol, constringndiff, constringpdiff, constringvia, constringpol
- QM1 -	CONRES		Contact resistors
			- constringppol, constringpol, constringndiff, constringpdiff, constringppol, constringpol
RS RM RL	CB	*	Cross bridges
			- cbm2, cbm1, cbpol
RS1 RM1 RL1	CB		Cross bridges
			- cbppol, cbm1, cbpol
SS SM SL	CB		Cross bridges
			- cbnd, cbpd, cbnfet
TS TM TL	CB		Cross bridges
			- cbnw, cbpw, cbpfet
US UM UL	ITHG		Italic H-gate
			- nl2w6ithg
VS VM VL	INVS		Inverters
			- inv3, inv4, inv5, inv6
WS WM WL	INVL		Inverters
			- inv7, inv8, inv9, inv10
- XM -	ALI	*	E-beam X-ray alignment structures - 4 $\mu$ m
			- m2vanpauw, m1vanpauw, alignviam1a, alignviam1b
- YM -	ALI	*	E-beam X-ray alignment structures - 4 $\mu$ m
			- m1avanpauw, polvanpauw, alignconpolya, alignconpolyb
- ZM -	ALI	*	E-beam X-ray alignment structures - 4 $\mu$ m

		- m1bvanpauw, ilvanpauw, - alignconila, alignconilb
- AaM -	NSQUARE	Unusually-sized <i>n</i> -channel MOSFETs 3/3, 4/4, 5/5, 6/6, 10/10, 20/20, 30/30, 6/30, 30/6
- BbM -	PSQUARE	Unusually-sized <i>p</i> -channel MOSFETs 3/3, 4/4, 5/5, 6/6, 10/10, 20/20, 30/30, 6/30, 30/6
- CcM -	KEYS	KEYS structures
- DdM -	BICMOS	Lateral bipolar structures - <i>npn</i> - base contact beside the emitter - implant all the way across
- EeM -	ALI	E-beam X-ray alignment structures - 8 $\mu\text{m}$ - poly/m1
- FfM -	ALI	E-beam X-ray alignment structures - 8 $\mu\text{m}$ - il/m1
- GgM -	BICMOS	Lateral bipolar structures - <i>pn</i> - base contact beside the emitter - implant all the way across
- HhM -	ALI	E-beam X-ray alignment structures - 8 $\mu\text{m}$ - ppoly/m1
- IiM -	BICMOS	Lateral bipolar structures - <i>npn</i> - base contact beside the emitter - implant 1/2 way across
- JjM -	BICMOS	Lateral bipolar structures - <i>pn</i> - base contact beside the emitter - implant 1/2 way across
- KkM -	BICMOS	Lateral bipolar structures - <i>npn</i> - base contact below gate - implant all the way across
- LlM -	BICMOS	Lateral bipolar structures - <i>pn</i> - base contact below gate - implant all the way across
- MmM -	BICMOS	Lateral bipolar structures - <i>npn</i> - base contact below gate - implant 1/2 way across
- NnM -	BICMOS	Lateral bipolar structures - <i>pn</i> - base contact below gate - implant 1/2 way across
- OoM -	BICMOS	Lateral bipolar structures - <i>npn</i> - like an <i>n</i> -channel MOSFET with the gate connected to the base
- PpM -	BICMOS	Lateral bipolar structures - <i>pn</i> - like a <i>p</i> -channel MOSFET with the

gate connected to the base

2. The 12 by 2 Modules -----

- aaM -	NODD	Unusually-sized <i>n</i> -channel MOSFETs
- bbM -	KEYS	KEYS structures (horizontal)

3. The 10 by 2 Modules -----

- AAM1 -	PROC	Processing structures
- aaaM -	NODD	Unusually-sized <i>n</i> -channel MOSFETs
- bbbM -	PODD	Unusually-sized <i>p</i> -channel MOSFETs
- cccM -	PODD	Unusually-sized <i>p</i> -channel MOSFETs

4. The 2 by 11 Module -----

- aaaaM -	KEYS	*	KEYS structures
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\* This module appears in the test library but not on NIST9.  
Also, no small modules appear on NIST9.

FOR THE 2 BY 16 MODULES:

S (Small)	L=0.2, 0.3, 0.4, 0.5, 0.6, 0.8 $\mu\text{m}$	
M (Medium)	L=2, 3, 4, 5, 6, 8 $\mu\text{m}$	W=6 $\mu\text{m}$
L (Large)	L=12, 13, 14, 15, 16, 18 $\mu\text{m}$	

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Table 10 - List of Large 10 by 7 Modules in the Test Library Organized by Function

MODULE	FUNCTION
CCM,CCM1 CCM2-CCM9	Capacitors - see tables 14 and 15
PPM-ZZM QQM1,TTM1,XXM1	Meanders - see table 13
DDM-MMM DDS-EES,DDL-EEL GGS-KKS,GGL-KKL	Dynamic circuits - see table 16
AAM	Processing structures
BBM	Circular, multi-edged, many-fingered, and regular MOSFETs
NNM,NNM1	Van der Pauw dopant resistivity test structures
OOM OOS,OOL	Multi-edge MOSFETs, multi-fingered MOSFETs, and italic H-gate MOSFETs
DLM	Threading dislocation structures
IRM	Suspended structures
DIO,DIO1	Meandering diodes

Table 11 - List of All But the Large 10 by 7 Modules in the Test Library  
Organized by Function

MODULE	FUNCTION
AM-KM,UM AS-CS,AL-CL ES-FS,EL-GL HS-JS,HL-JL US,UL	MOSFETS - see table 12
LM-QM PM1,QM1	Contact resistors
RM-TM RS-TS, RL-TL RS1,RM1,RL1	Cross-bridges
VM-WM VS-WS, VL-WL	Inverters
XM-ZM EeM, FfM, HhM	E-beam x-ray alignment structures
AaM, BbM aaM, aaaM, bbbM, cccM	Unusually-sized MOSFETs
CcM, bbM, aaaaM	KEYS structures
DdM, GgM IiM, JjM KkM, LlM MmM, NnM OoM, PpM	Lateral bipolar structures
AAM1	Processing structures

Table 12 - List of Modules Consisting of MOSFETs Found in the Test Library with a Sample Subcell Name Given

MODULE S M L	FUNCTION	SAMPLE SUBCELL NAME
AS AM AL	<i>n</i> -channel MOSFETs	nl2w6
- GM GL	<i>n</i> -channel MOSFETs with a source-to-channel tie	nl2w20tie
CS CM CL	minimum sized <i>n</i> -channel MOSFETs	nl2w6min
BS BM BL	<i>p</i> -channel MOSFETs	pl2w6
HS HM HL	depletion-mode MOSFETs	dl2w6
- DM -	circular <i>n</i> - and <i>p</i> -channel MOSFETs	nl6w82circ
- KM -	circular <i>n</i> - and <i>p</i> -channel MOSFETs with no channel contact	nl6w82circnoc
ES EM EL	H-gate <i>n</i> -channel MOSFETs	nl2w20hg
IS IM IL	H-gate <i>n</i> -channel MOSFETs with a source-to-channel tie	nl2w20hgtie
US UM UL	<i>italic</i> H-gate <i>n</i> -channel MOSFETs	nl2w6ithg
FS FM FL	T-gate <i>n</i> -channel MOSFETs	nl2w20tg
JS JM JL	T-gate <i>n</i> -channel MOSFETs with a source-to-channel tie	nl2w20tgtie
AaM, aaM, aaaM	unusually-sized <i>n</i> -channel MOSFETs	
BbM, bbbM, cccM	unusually-sized <i>p</i> -channel MOSFETs	



Table 13 - List of Modules Consisting of Meanders Found in the Test Library

TYPE OF MEANDER	MODULE	LAYER(S) INVOLVED
1. INDIVIDUAL MEANDERS - checks for shorts and opens at corners and along straight lines for horizontal and vertical alignments		
- Kelvin measurements are possible		
- 597 corners for the 8- $\mu$ m meander		
- 567 corners for the 3-, 4-, and 6- $\mu$ m meanders		
	PPM	island
	QQM	poly
	QQM1	ppoly
	RRM	m1
	SSM	m2
2. STEP COVERAGE MEANDERS - checks for step coverage, shorts, and continuity for horizontal and vertical alignments		
- for two levels that do NOT have a contact between them		
- 1631 crossings		
	TTM	poly/il
	TTM1	ppoly/il
	UUM	m2/il
	VVM	m2/poly
3. CONTACT MEANDERS - tests step coverage, tests the integrity of the glass between the two layers, detects shorts between the two layers, and checks continuity for horizontal and vertical alignments		
- for two levels that DO have a contact between them		
- 1232 contacts		
	WWM	m1/il
	XXM	m1/poly
	XXM1	m1/ ppoly
	YYM	m2/m1
4. SUBSTRATE CONTACT MEANDER - tests continuity of metal1 into a substrate contact (horizontal and vertical alignments are considered)		
- 993 contacts		
	ZZM	sub

Table 14 - Capacitors on Modules CCM and CCM1 Found in the Test Library

LAYER1	LAYER2	SUBCELL NAME	MODULE
m2	m1	capm1m2 (over il)	CCM
	poly	capm2pol (over il)	CCM
	il	capm2il	CCM
	sub	capm2	CCM
m1	poly	capm1pol (over il)	CCM
	ppoly	capm1ppol (over il)	CCM1
	il	capm1il	CCM
	sub (without il)	capm1	CCM
poly	il	cappolil	CCM
		cappolnw	CCM1
		cappolpw	CCM1
		capchann	CCM1
	nwell/ nndiff	capchanp	CCM1
	sub (without il)	cappol	CCM
ppoly	il	capppolil	CCM1
	sub (without il)	capppol	CCM1
il	sub	capil	CCM
		capnw	CCM1
		cappw	CCM1
		capn	CCM1
		capp	CCM1

The capacitance can be calculated using the equation:

$$C \text{ (in pF)} = \epsilon_{ox}(A)/t_{ox}$$

where

$$\epsilon_{ox} = 8.85e-6 \text{ pF}/\mu\text{m}$$

$$A = \text{area in } \mu\text{m}^2$$

$$t_{ox} \text{ in } \mu\text{m}$$

Table 15 - Capacitors on Modules CCM2 through CCM9 Found in the Test Library

LAYER1	LAYER2	DIMENSIONS		MODULE
m1	poly	(1300x775 $\mu\text{m}^2$ )	18 pF with tox=5000 Å	CCM3
	ppoly	(1300x775 $\mu\text{m}^2$ )	18 pF with tox=5000 Å	CCM5
	il	(1300x775 $\mu\text{m}^2$ )	22 pF with tox=4000 Å	CCM3
	sub	(1312x1530 $\mu\text{m}^2$ )	22 pF with tox=8000 Å	CCM2
	poly/il/sub	(1312x1530 $\mu\text{m}^2$ )		CCM7
	ppoly/il/sub	(1312x1530 $\mu\text{m}^2$ )		CCM8
poly	il	(625x775 $\mu\text{m}^2$ )	86 pF with tox=500 Å	CCM6,9
	sub	(1300x775 $\mu\text{m}^2$ )	22 pF with tox=4000 Å	CCM4
	nndiff	(625x775 $\mu\text{m}^2$ )	tox=500 Å	CCM9
	ppdiff	(625x775 $\mu\text{m}^2$ )	tox=500 Å	CCM9
ppoly	il	(625x775 $\mu\text{m}^2$ )	86 pF with tox=500 Å	CCM6,9
	sub	(1300x775 $\mu\text{m}^2$ )	22 pF with tox=4000 Å	CCM5
	nndiff	(625x775 $\mu\text{m}^2$ )	tox=500 Å	CCM6
	ppdiff	(625x775 $\mu\text{m}^2$ )	tox=500 Å	CCM6
il	sub	(1300x775 $\mu\text{m}^2$ )	22 pF with tox=4000 Å	CCM4

The capacitance can be calculated using the equation:

$$C \text{ (in pF)} = \text{eox}(A)/\text{tox}$$

where

$$\text{eox} = 8.85\text{e-}6 \text{ pF}/\mu\text{m}$$

$$A = \text{area in } \mu\text{m}^2$$

$$\text{tox in } \mu\text{m}$$

The capacitor areas have been adjusted such that the capacitance is greater than 10 pF.



Table 16 - List of Modules Containing Dynamic Circuits Found in the Test Library with a Sample Subcell Name Given

DYNAMIC CIRCUIT	MODULE S M L			SAMPLE SUBCELL NAME	MOSFETS USED
RING OSCILLATORS					
	EES	EEM	EEL	amp	<i>n</i> - and <i>p</i> -channel MOSFETs
	IIS	IIM	IIL	amptie	MOSFETs with source-to-channel ties
	-	FFM	-	ampcirc	circular MOSFETs with channel contacts
	-	LLM	-	ampcircnoc	circular MOSFETs with no channel contacts
	GGs	GGM	GGL	amphg	H-gate MOSFETs
	JJS	JJM	JJL	amphgtie	H-gate MOSFETs with source-to-channel ties
	HHS	HHM	HHL	amptg	T-gate MOSFETs
	KKS	KKM	KKL	amptgtie	T-gate MOSFETs with source-to-channel ties
STATIC RAMS					
	DDS	DDM	DDL	sramcell	<i>n</i> - and <i>p</i> -channel MOSFETs
	-	MMM	-	sramcellcirc	circular MOSFETs

Table 17 - Organization of the Modules on NIST8

	C1 AM NCHAN	C2 BM PCHAN	C3 CM NMIN	C4 DM CIRC	C5 KM CIRCNO	C6 EM HG	C7 UM ITHG	C8 FM TG	C9 VM INV	C10 XM ALI	C11 AaM NSQ
R1	L2 W6 N	L2 W6 P	L2 W6 N	L6 W82 N	L6 W82 N	L2 W20 N	L2 W6 N	L2 W20 N	L3		L3 W3 N
R2	L3 W6 N	L3 W6 P	L3 W6 N	L9 W79 N	L9 W79 N	L3 W20 N	L3 W6 N	L3 W20 N			L4 W4 N
R3	L4 W6 N	L4 W6 P	L4 W6 N	L12 W107 N	L12 W107 N	L4 W20 N	L4 W6 N	L4 W20 N	L4		L5 W5 N
R4	L5 W6 N	L5 W6 P	L5 W6 N	L6 W82 P	L6 W82 P	L5 W20 N	L5 W6 N	L5 W20 N	L6		L8 W8 N
R5	L6 W6 N	L6 W6 P	L6 W6 N	L9 W79 P	L9 W79 P	L6 W20 N	L6 W6 N	L6 W20 N			L10 W10 N
R6	L8 W6 N	L8 W6 P	L8 W6 N	L12 W107 P	L12 W107 P	L8 W20 N	L8 W6 N	L8 W20 N	L10		L30 W30 N
R7	L6 W3 N	L6 W4 N	NODD aaM	L6 W5 N	L6 W8 N	L50 W50 N	L6 W10 N	L10 W6 N	NODD aaaM	L6 W30 N	L30 W6 N
R8	R9C3 SRAM DDM					L3 W3 P	R9C9 RING23 EEM				
R9						PSQU L4 W4 P					
R10	L6 W3 P	L6 W4 P	P0DD bbbM	L6 W5 P	L6 W8 P	L5 W5 P	L6 W10 P	L10 W6 P	P0DD cccM	L6 W30 P	L30 W6 P
R11	R12C3 RINGHG GGM					L8 W8 P	-	00M	-	NXTORS	-
R12						BbM L10 W10 P	L20 W120	-	L20 W1760	-	L20 W120
R13						L30 W30 P	L20 W80	-	L20 W1320	-	L20 W80

Table 18 - Method Used To Get Submicrometer Dimensions on NIST8

---

1.	Check CIF file for everything except submicrometer dimensions		
	\$ cd nist8100	nist8.mag	1x
	\$ magic nist8	nist8.cif	1x
	cif1x (MOSIS)		
	:quit		
	\$ magic -Tsimox blank		
	cif istyle 1x (MOSIS)		
	:cif read nist8		
	CHECK CIF		
	:quit		

---

2.	Make submicrometer file		
	\$ cd nist8100		
	\$ magic nist8		
	cif1x (MOSIS)		
	:quit		
	\$ magic -Tsimox blank		
	:cif istyle mosis(SCE)in10x		
	:cif read nist8		
	f,z		
	:load nist8		
	edit to proper dimensions (the whole hierarchy)		
	:edit		
	:save alignviam100		
	:edit		
	:save xm100		
	:edit		
	:save nist8100	(of selected files) nist8100.mag	10x
	:cif ostyle out-10x		
	:cif write nist8100	(send this) nist8100.cif	1x
	:quit		

---

3.	Check the CIF file to be sent		
	\$ magic -Tsimox blank		
	cif istyle 1x (MOSIS)		
	:cif read nist8100		
	CHECK CIF (especially submicrometer dimensions)		
	:quit		

---

4.	Check for submicrometer dimensions		
	\$ vi nist8100.cif		
	/alignviam1		

---



Table 19 - Organization of the Large 10 by 7 Modules on NIST9

PRELIMINARY CALCULATIONS:

1 processing	x2= 2 + 2 inside
1 B module	x2= 2
8 capacitors	x2=16
10 medium rings/srams	x2=20
7 large rings/srams	x2=14
2 van der Pauw	x2= 4
2 O modules	x2= 4
10 meanders	x2=20
1 threading	x2= 2
1 suspended	x4= 4 + 2 inside
2 diodes	x2= 4
-----	
Total modules	92 + 4 inside
Possible slots	92

NUM MODULES SIZE			ABBREVIATED PLACEMENTS (e.g., A=AAM, K=KKM) ABBREVIATED DESCRIPTION (e.g., pr=processing)														
14 MISC M	-	-	C6 c	A pr	E rings(M)	F	G	H	I	J	K	L	D	M	B	A pr	
14 MISC L	-	-	C5 c	IR ir	DL dl	E rings(L)	G	H	I	J	K	D	OM	OL	N	N1 vp....	
16 MISC M	B	C7 c	DI diodes..	DI1	P meanders	Q	Q1	R	T	T1	W	X	X1	Z	C7	C5 caps..	
16 M	OM	C2 caps.....	C4	C9	E rings(M)	F	G	H	I	J	K	L	D	M	C3	C8 caps..	
16 L	OL	N vp	C3 caps....	C8	IR rings(L)	E	G	H	I	J	K	D	IR	C6	C2	C9 caps.....	
16 MISC	DL dl	N1 vp	DI diodes..	DI1	P meanders	Q	Q1	R	T	T1	W	X	X1	Z	C4	IR ir	

Table 20 - Organization of All the Modules Except the Large 10 by 7 Modules on NIST9

PRELIMINARY CALCULATIONS:

```

22 MOSFETs (M + L)          106 modules
   6 contact resistors (M)    x 3 iterations
   6 cross bridges (M + L)    -----
   4 inverters (M + L)        318 modules
   3 e-beam structures (M)     382 possible spaces
   2 unusually-sized (M)       -----
10 bipolar (M)                64 extra spaces
-----                       -46 KEYS only
53 total modules              -----
53 KEYS modules interleaved   18 extra spaces for MOSFETs/KEYS
-----                       so 9 extra MOSFET modules
06 modules

```

Therefore the abbreviated sequencing (e.g., A=AM, U=UM) is:

A-K,U, MOSFETs	V,W, inv	Aa,Bb, square	Dd,Gg,Ii-Pp, bipolar	L-T, cr,cb	Ee,Ff,Hh x-ray
-------------------	-------------	------------------	-------------------------	---------------	-------------------

NOTES:

1. KEYS modules alternate with the 2 by 16 modules (top to bottom)  
(There are 3+ repetitions of the 2 by 16 modules)

4K4K4K4K

3K3K3K3K3K3K4K4K4K

3K3K3K3K3K3K3K3K3K3K3K3K3K3K3K3K

3K

**3K3K3K3K3K3K3K3K3K3K3K3K3K2K2K2K2K2K2K2K2K2K**

2K2

[illegible][illegible]

4K4K-K-K-K-K-K-K-K-K-K-K-K-K-K-K-K-K

K-K-K-K-K-K-K-K-K-K-K-K-K-K-K-K-K-K

K-K-K-K-K-K-K-K-K-K-K-K-K-K-K-K

2. AAM1 appears below each AAM processing module
3. Horizontal modules (top to bottom)

- ```

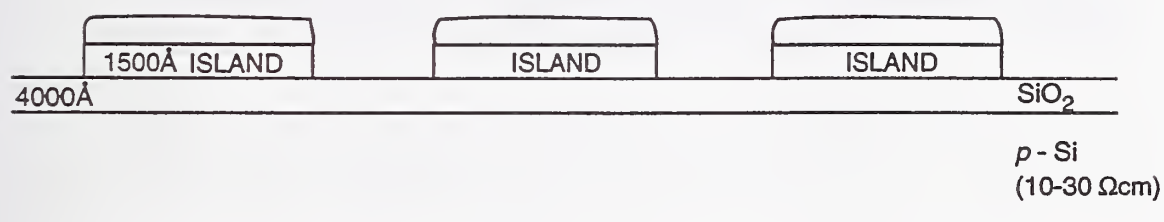
2 KEYS (bbM)
4 KEYS
5 KEYS
7 KEYS
8 KEYS
10 KEYS
12 KEYS
13 KEYS
12 cccM, 2 AAM1
15 KEYS
16 aaaM
16 KEYS
16 bbbM
16 aaM

```

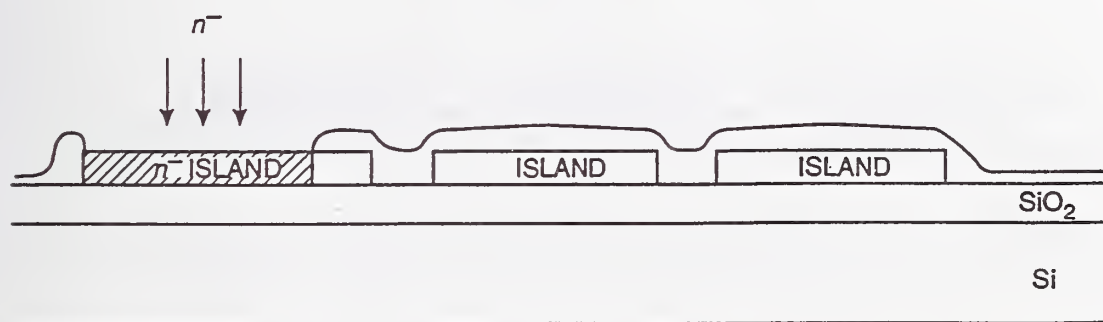
4. Border problem files = OM, XM, YM, ZM, EeM, FfM, HhM  
CCM3, CCM4, CCM5, CCM6, CCM9, WWM, XXM, XXM1, YYM, ZZM

APPENDIX A — Sideviews of the 14 SIMOX Processing Mask Steps  
Used to Fabricate NIST9

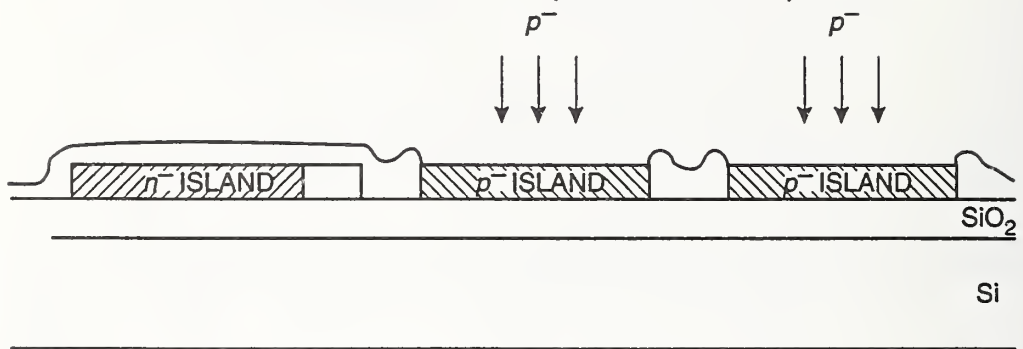
STEP 1 - ISLAND (a clear field mask)



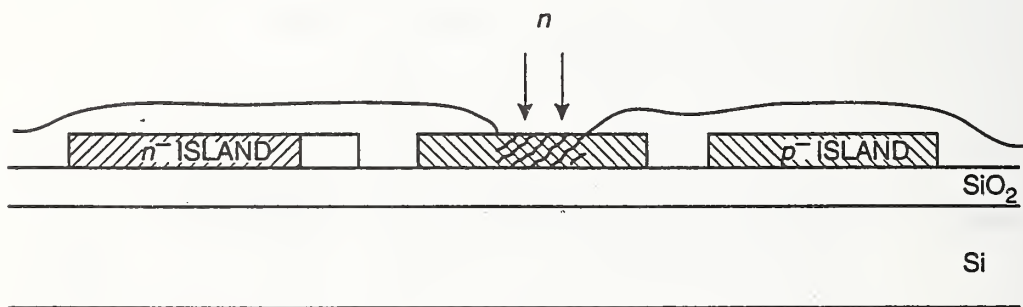
STEP 2 - NWELL (a dark field mask)



STEP 3 - PWELL (a dark field mask)

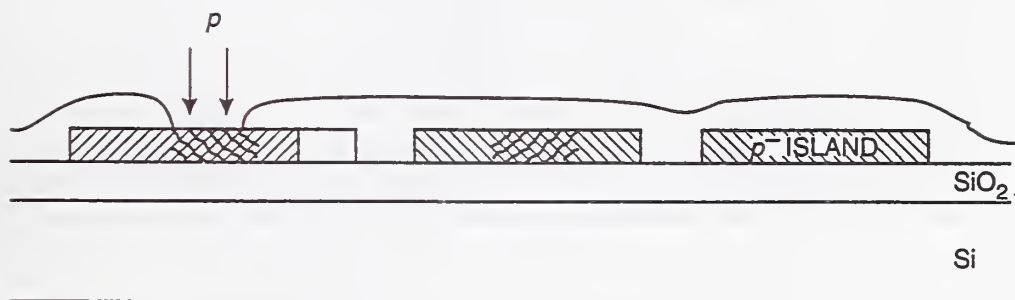


STEP 4 - NTIE IMPLANT (a dark field mask)

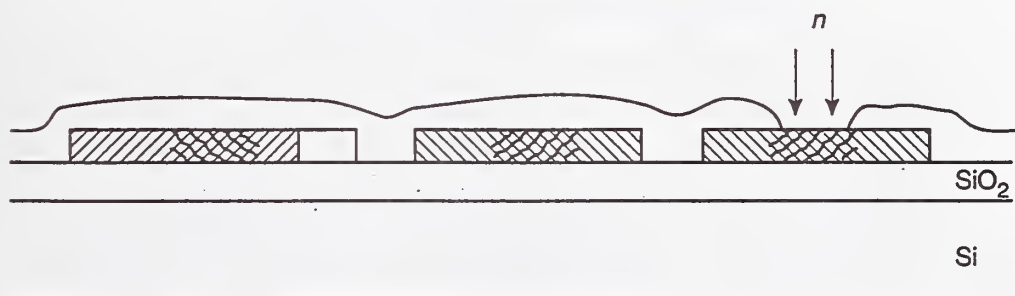




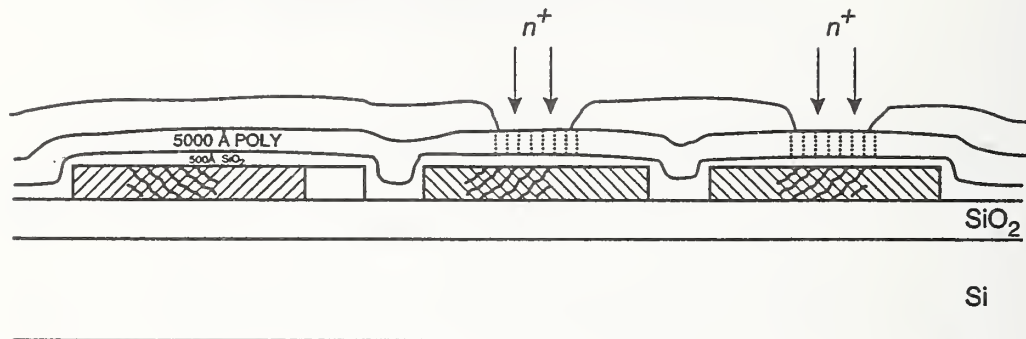
STEP 5 - PTIE IMPLANT (a dark field mask)



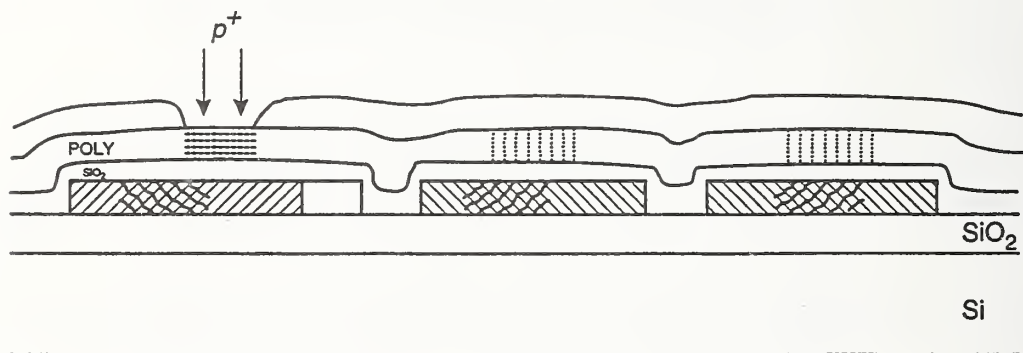
STEP 6 - DFET IMPLANT (a dark field mask)



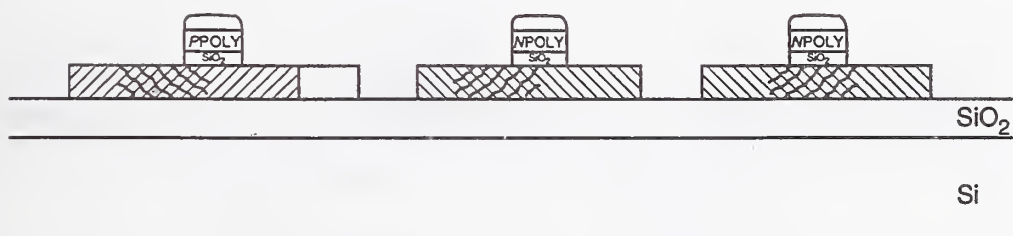
STEP 7 - NPOLY IMPLANT



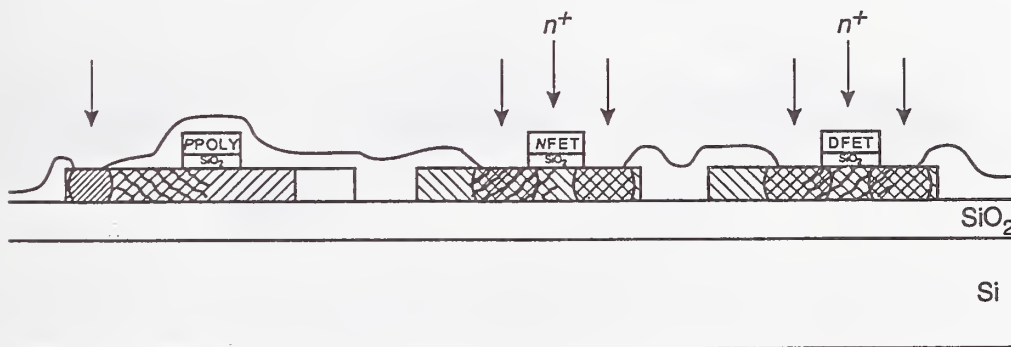
STEP 8 - PPOLY IMPLANT



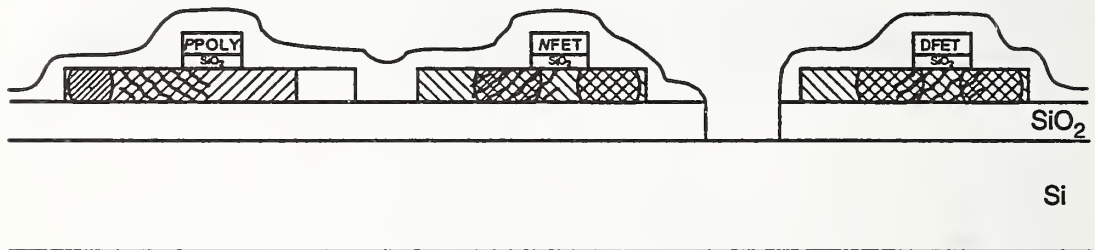
STEP 9 - POLYSILICON (a clear field mask)



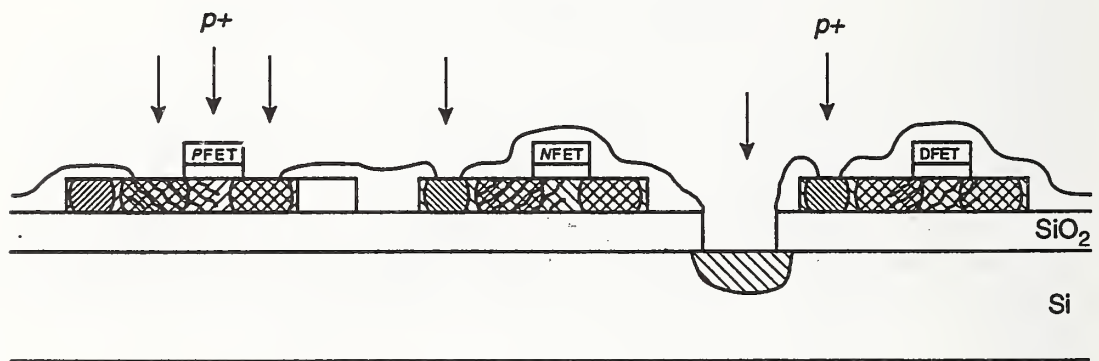
STEP 10 - NIMPLANT (a dark field mask)



STEP 11 - SUBSTRATE CONTACT (a dark field mask)

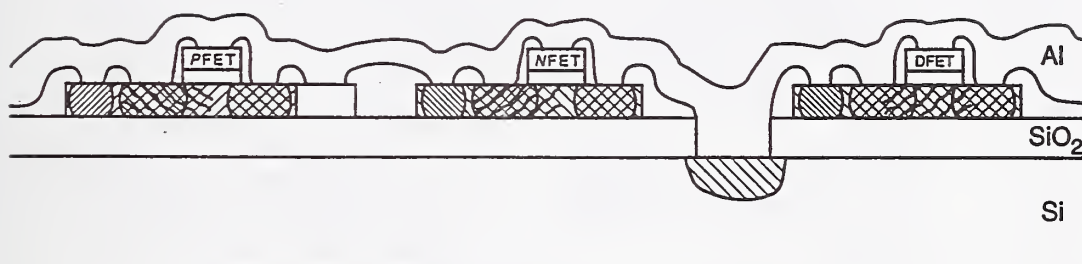


STEP 12 - PIMPLANT (a dark field mask)

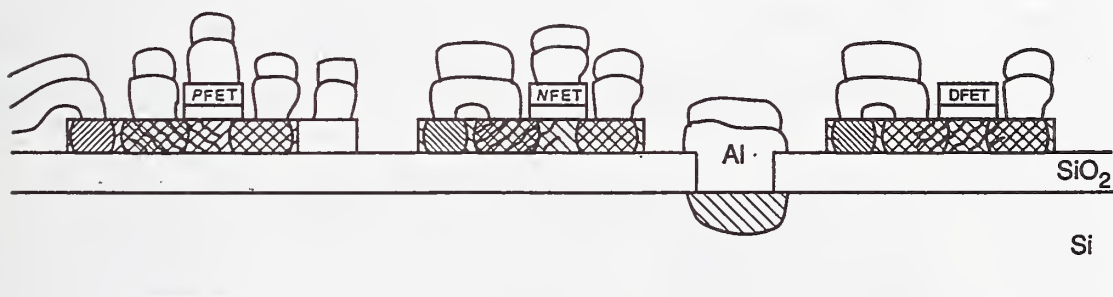




STEP 13 - CONTACTS (a dark field mask)



STEP 14 - METAL (a clear field mask)



# APPENDIX B — Abbreviated SOI/SIMOX Technology File

```
/* ----- *
* simox.tech -- The SIMOX Technology File for lambda=1.0      *
* ----- */
```

```
types /* tiles */
```

```
/* primary layers */
```

|        |                                   |
|--------|-----------------------------------|
| glass  | glass                             |
| glass  | open                              |
| metal3 | metal2c,metal3,m2c,via,m2contact  |
| metal2 | metal2,m2,purple                  |
| metal1 | metal1,m1,blue                    |
| active | polysilicon,red,poly,p,npoly      |
| active | ppoly                             |
| glass  | etch,netch                        |
| glass  | petch                             |
| active | ndiffusion,green,ndiff            |
| active | pdiffusion,brown,pdiff            |
| active | ndiff                             |
| active | ppdiff                            |
| metal2 | ntie,nbody_tie,n_xtor_bodytie,tie |
| metal2 | ptie,pbody_tie,p_xtor_bodytie     |
| well   | nwell,nw                          |
| well   | pwell,pw                          |
| metal2 | dimplant                          |
| island | island,il,yellow                  |
| island | pad                               |
| island | ppad                              |
| island | substrate,subst                   |
| active | legend                            |
| well   | legb,legend_background            |

```
/* Contacts */
```

|        |                         |
|--------|-------------------------|
| active | polycontact,pcontact,pc |
| active | ppolycontact,ppc        |
| active | ndpcontact,ndpc         |
| active | pdpcontact,pdpc         |
| active | ndcontact,ndc           |
| active | pdcontact,pdc           |
| active | nwcontact,nwc           |
| active | pwcontact,pwc           |
| glass  | hole,contact            |
| metal1 | ilcontact,ilc           |
| metal1 | subcon                  |

```
/* Transistors */
```

|        |                  |
|--------|------------------|
| active | ntransistor,nfet |
|--------|------------------|

```

active      ptransistor,pfet
active      dtransistor,dfet

```

```
end
```

```

#define allMetal2 m2,m2c
#define allSomeM1 m1,pc/m1,ppc,ndpc/m1,pdpc/m1,ndc/m1,pdc/m1
#define allMetal1 allSomeM1,nwc/m1,pwc/m1,ilc/m1,subcon/m1
#define allPoly1 poly,pc/active,ppc,nfet,dfet,ndpc/active
#define allPoly allPoly1,ppoly,pfet,pdpc/active
#define allNpoly poly,pc/active,nfet,dfet,ndpc/active
#define allPpoly ppoly,ppc,pfet,pdpc/active
#define allNdiff ndiff,ndc/active,nndiff,nwc/active,nfet,dfet,ndpc/active
#define allPdiff pdiff,pdc/active,ppdiff,pwc/active,pfet,pdpc/active
#define allSomeD ndiff,pdiff,ndc/active,pdc/active,ndpc/active,pdpc/active
#define allDiff allSomeD,nndiff,ppdiff,nwc/active,pwc/active,nfet,pfet
#define allDiff0 nndiff,ppdiff,nwc/active,pwc/active
#define allNwell nw,nwc/active
#define allPwell pw,pwc/active
#define allIsland il,ilc/il
#define allSub subst,subcon/subst

```

```
cifoutput
```

```
style photronix
```

```

scalefactor 100
layer SWN allNwell
  calma 2 1
layer SWP allPwell
  calma 3 1
layer SIL allIsland,pad,ppad
  calma 1 1
layer SMF pad,ppad
  shrink 400
  or allMetal1
  grow 200
  shrink 200
  calma 14 1
layer SPG pad,ppad
  shrink 200
  or allNpoly,allPpoly,etch,petch
  grow 100
  shrink 100
  calma 7 1
layer SNP pad
  shrink 200
  or allNpoly,etch
  grow 100
  shrink 100
  calma 8 1

```

```

layer SPP ppad
    shrink 200
    or allPoly,etch
    grow 100
    shrink 100
    calma 9 1
layer SND allNdiff
    calma 10 1
layer SPD allPdiff
    calma 12 1
layer SNT ntie
    calma 4 1
layer SPT ptie
    calma 5 1
layer SDF dfet
    grow 200
    or dimplant
    calma 6 1
layer SCT subcon,pad,ppad
    shrink 800
    or ndc,pdc,nwc,pwc,pc,ppc,ilc,ndpc,pdpc
    shrink 200
    or open,hole
    calma 13 1
layer SCS subcon,substrate,open
    calma 11 1
/* layer SOG pad,ppad
    shrink 600
    or glass,open
    calma 15 1
*/

style mosis(SCE)out1x
scalefactor 100
layer CWN allNwell
    calma 1 1
layer CWP allPwell
    calma 2 1
layer CMS pad
    shrink 400
    or allMetal2
    calma 3 1
layer CMF pad
    shrink 200
    or allMetal1,m2c
    calma 4 1
layer CPG allPoly,pad
    calma 5 1
layer CAA allNdiff,allPdiff
    and allIsland

```



```

    calma 6 1
layer CVA m2c
    shrink 100
    calma 7 1
layer CVA pad
    shrink 500
    calma 7 1
layer CSN ndiff,nfet
    grow 200
    or allNdiff
    calma 8 1
layer CSP pdiff,pfet
    grow 200
    or allPdiff
    calma 9 1
layer CCA ndc,pdc,pwc,nwc
    shrink 200
    calma 10 1
layer CCP pc,ndpc,pdpc
    shrink 200
    calma 11 1
layer CCP pad
    shrink 300
    calma 11 1
layer COG pad
    shrink 600
    or glass
    calma 12 1

```

end

cifinput

```

style photronix
scalefactor 100
layer nw SWN
layer pw SWP
layer m1 SMF
layer poly SNP
layer ppoly SPP
layer ndiff SND
layer pdiff SPD
layer nndiff SND
    and SWN
layer ppdiff SPD
    and SWP
layer ndiff SND
    and-not SWN
layer pdiff SPD
    and-not SWP
layer ntie SNT

```

layer ptie SPT  
layer nfet SPG  
    and SND  
    and-not SWN  
layer pfet SPP  
    and SPD  
    and-not SWP  
layer dfet SPG  
    and SND  
    and SDF  
layer dimplant SDF  
    and-not SPG  
layer etch SPG  
    and SND  
    and SWN  
layer petch SPG  
    and SPD  
    and SWP  
layer hole SCT  
    and-not SMF  
layer ilc SCT  
    and SIL  
    and SMF  
layer ndc SCT  
    and SND  
    and SMF  
    and SIL  
layer pdc SCT  
    and SPD  
    and SMF  
    and SIL  
layer nwc SCT  
    and SND  
    and SWN  
    and SMF  
    and SIL  
layer pwc SCT  
    and SPD  
    and SWP  
    and SMF  
    and SIL  
layer pc SCT  
    and SPG  
    and SMF  
    and-not SND  
    and-not SPD  
layer ppc SCT  
    and SPP  
    and SMF

```

        and-not SND
        and-not SPD
    layer ndpc SCT
        and SPG
        and SMF
        and SND
    layer pdpc SCT
        and SPP
        and SMF
        and SPD
    layer il SIL
    layer substrate SCS
        and-not SCT
    layer subcon SCT
        and SCS
        and SMF
    layer ppoly SPP
        and-not SWP
/*    layer glass SOG
*/

    layer open SCT
        and SCS
        and-not SMF
        and-not SPD
/*    and SOG
*/

calma SWN 2 *
calma SWP 3 *
calma SIL 1 *
calma SMF 14 *
calma SPG 7 *
calma SNP 8 *
calma SPP 9 *
calma SND 10 *
calma SPD 12 *
calma SNT 4 *
calma SPT 5 *
calma SDF 6 *
calma SCT 13 *
calma SCS 11 *
/*    calma SOG 15 *
*/

style mosis(SCE) in1x
scalefactor 100
layer nw CWN
layer pw CWP
layer m2c CVA
layer m2 CMS

```

layer m1 CMF  
layer poly CPG  
layer il CAA  
layer nndiff CSN  
    and CWN  
layer ppdiff CSP  
    and CWP  
layer ndiff CSN  
    and-not CWN  
layer pdiff CSP  
    and-not CWP  
layer nfet CPG  
    and CAA  
    and CSN  
layer pfet CPG  
    and CAA  
    and CSP  
layer pdc CCA  
    and CAA  
    and CSP  
    and CMF  
layer ndc CCA  
    and CAA  
    and CSN  
    and CMF  
layer pwc CCA  
    and CAA  
    and CSP  
    and CMF  
    and CWP  
layer nwc CCA  
    and CAA  
    and CSN  
    and CMF  
    and CWN  
layer pc CCP  
    and CPG  
    and CMF  
    and-not CSN  
    and-not CSP  
layer ndpc CCP  
    and CPG  
    and CMF  
    and CSN  
layer pdpc CCP  
    and CPG  
    and CMF  
    and CSP  
layer glass COG

end



## APPENDIX C — Test Algorithm KEYSiv

```

10  !
20  ! APPENDIX C -- Test algorithm KEYSiv (the program used to obtain the IV
30  ! data points on NIST8)
40  !
50  SUB Keysiv_mos(W$,R$,C$,INTEGER Pins(*),REAL Width,Length,Type$,Vgs(*),Vds(
60  Keysiv_mos: !*****
70  !
80  ! RE-STORE "/users/marshall/icms/ALG/BASIC/Keysiv_MOS"
90  !
100 ! LOADSUB ALL FROM "/usr/pcs/lib/XYGRAPH"
110 !
120 !*****
130 !
140 ! Programmers : Janet Marshall
150 !
160 ! Date : 04/20/1992 12:35:45
170 ! Revised : 04/20/1992 12:35:45
180 ! Device Class : MOSFET
190 ! Description : Mosfet drain current measurement at specified
200 ! : Vds,Vgs,Vbs and Vss.
210 ! Procedure :
220 !
230 ! Input Variables:
240 !
250 ! # Name Type Size Description
260 ! ---
270 ! Measurement Parameters:
280 ! 1 W S - Wafer Letter
290 ! 2 R S - Row Number
300 ! 3 C S - Column Number
310 !
320 ! Device Terminals:
330 ! 1 Gate I - Gate terminal
340 ! 2 Drain I - Drain terminal
350 ! 3 Source I - Source terminal
360 ! 4 Bulk I - Bulk terminal
370 ! 5 Sub I - Substrate contact
380 ! 6 Chuck I - Wafer chuck
390 !
400 ! Device Parameters:
410 ! 1 Width R - um, Mask channel width
420 ! 2 Length R - um, Mask channel length
430 ! 3 Type C - Channel type (P/N)
440 !
450 ! Output Variables:
460 !
470 ! # Name Type Size Description
480 ! ---
490 ! Output Parameters:
500 ! 1 Vgs A 13 Gate Voltage
510 ! 2 Vds A 13 Drain Voltage
520 ! 3 Ids1 A 13 Drain Current(1)
530 ! 4 Ids2 A 13 Drain Current(2)
540 ! 5 Ids3 A 13 Drain Current(3)
550 ! 6 Vbs R - Substrate Voltage
560 !
570 !*****
580 !
590 !
600 ! INPUT "Number of points in a sweep = ",M

```

```

610 M=13
620 OPTION BASE 1
630 !
640 INTEGER Gate, Drain, Source, Substrate, Line, I, K, M, N, P, Q, T, Current
650 INTEGER Number1, Number2
660 REAL Vsource
670 !
680 ALLOCATE Ids(M), Id(13, M)
690 DIM Vds1(3), Vds2(10), Id1(3), Id2(10)
700 DIM Vgate_min(3), Vgate_max(3), Vgate_step(3)
710 DIM Start(3), Stop(3)
720 DIM File$(40), Dir$(40), Concat$(40)
730 DIM String_1$(40), String_2$(40), String_3$(40)
740 DIM String_4$(40), String_5$(40), String_6$(40)
750 DIM Y$(2), Z$(1)
760 !
770 !=====
780 !
790 ! Determine the filename
800 !
810 !PRINT "C$ = ", C$
820 !PRINT "Y$ = ", Y$
830 !PRINT "Z$ = ", Z$
840 !
850 R$="0"
860 IF Length=2.0 THEN R$="1"
870 IF Length=3.0 AND (Width=6.0 OR Width=20.0) THEN R$="2"
880 IF Length=4.0 AND (Width=6.0 OR Width=20.0) THEN R$="3"
890 IF Length=5.0 AND (Width=6.0 OR Width=20.0) THEN R$="4"
900 IF Length=6.0 AND (Width=6.0 OR Width=20.0) THEN R$="5"
910 IF Length=8.0 AND (Width=6.0 OR Width=20.0) THEN R$="6"
920 !
930 IF Width=82. AND Type$="N" THEN R$="1"
940 IF Width=82. AND Type$="P" THEN R$="4"
950 IF Width=79. AND Type$="N" THEN R$="2"
960 IF Width=79. AND Type$="P" THEN R$="5"
970 IF Width=107. AND Type$="N" THEN R$="3"
980 IF Width=107. AND Type$="P" THEN R$="6"
990 !
1000 IF Type$="P" THEN GOTO 1270
1010 !
1020 ! N-channel devices
1030 !
1040 IF Length=Width AND Length=3. THEN R$="1"
1050 IF Length=Width AND Length=4. THEN R$="2"
1060 IF Length=Width AND Length=5. THEN R$="3"
1070 IF Length=Width AND Length=8. THEN R$="4"
1080 IF Length=Width AND Length=10. THEN R$="5"
1090 IF Length=Width AND Length=30. THEN R$="6"
1100 IF Length=Width AND Length=50. THEN R$="7"
1110 IF Length=Width AND Length=50. THEN C$="6"
1120 !
1130 IF R$="0" THEN R$="7"
1140 !
1150 IF R$="7" AND Width=3. THEN C$="1"
1160 IF R$="7" AND Width=4. THEN C$="2"
1170 IF R$="7" AND Width=5. THEN C$="4"
1180 IF R$="7" AND Width=8. THEN C$="5"
1190 IF R$="7" AND Width=10. THEN C$="7"
1200 IF R$="7" AND Length=10. THEN C$="8"

```

```

1210 IF R$="7" AND Width=30. THEN C$="10"
1220 IF R$="7" AND Length=30. THEN C$="11"
1230 GOTO 1490
1240 !
1250 ! P-channel devices
1260 !
1270 IF Length=Width AND Length=3. THEN R$="8"
1280 IF Length=Width AND Length=4. THEN R$="9"
1290 IF Length=Width AND Length=5. THEN R$="10"
1300 IF Length=Width AND Length=8. THEN R$="11"
1310 IF Length=Width AND Length=10. THEN R$="12"
1320 IF Length=Width AND Length=30. THEN R$="13"
1330 IF R$="10" THEN GOTO 1610
1340 !
1350 IF R$="0" THEN R$="10"
1360 !
1370 IF R$="10" AND Width=3. THEN C$="1"
1380 IF R$="10" AND Width=4. THEN C$="2"
1390 IF R$="10" AND Width=5. THEN C$="4"
1400 IF R$="10" AND Width=8. THEN C$="5"
1410 IF R$="10" AND Width=10. THEN C$="7"
1420 IF R$="10" AND Length=10. THEN C$="8"
1430 IF R$="10" AND Width=30. THEN C$="10"
1440 IF R$="10" AND Length=30. THEN C$="11"
1450 GOTO 1610
1460 !
1470 ! Chip OOM
1480 !
1490 IF C$<>"0" THEN GOTO 1610
1500 IF Width=120 OR Width=1760 THEN R$="12"
1510 IF Width=80 OR Width=1320 THEN R$="13"
1520 IF Width>1000 THEN C$="9"
1530 !
1540 IF Pins(2)=18 OR Pins(1)=8 THEN C$="7"
1550 IF Pins(2)=46 OR Pins(2)=48 THEN C$="11"
1560 !PRINT "Pins(2)=";Pins(2)
1570 !PRINT "Pins(1)=";Pins(1)
1580 !
1590 !=====
1600 !
1610 Dir$="/users/marshall/nist8data/"
1620 !
1630 File$=Type$&"W"&W$&"R"&R$&"C"&C$&".DAT"
1640 !
1650 Concat$=Dir$&File$
1660 !
1670 !PRINT Concat$
1680 !
1690 !-----
1700 !
1710 ! Specify default mass storage
1720 !
1730 !MASS STORAGE IS ":",600,1"
1740 !
1750 ! Create ASCII data file with 10 sectors on the specified
1760 ! mass storage device (:,600,1)
1770 !
1780 ON ERROR GOTO File_exists
1790 CREATE ASCII Concat$,10
1800 File_exists: OFF ERROR

```

```

1810      !
1820      ! Assign (or open) an I/O path name to the file
1830      !
1840      ASSIGN @Path_1 TO Concat$
1850      !
1860      !-----
1870      !
1880      Init_system
1890      !
1900      ! Define measurement pins
1910      !
1920      Gate=Pins(1)
1930      Drain=Pins(2)
1940      Source=Pins(3)
1950      Substrate=Pins(4)
1960      !
1970      ! Connect pins to sources
1980      !
1990      Connect(FNSmu(1),Drain)
2000      Connect(FNSmu(2),Gate)
2010      Connect(FNGnd,Source)
2020      Connect(FNSmu(3),Substrate)
2030      !
2040      ! Force bias conditions
2050      !
2060      IF Type$="N" THEN S=1.0
2070      IF Type$="P" THEN S=-1.0
2080      !
2090      Vsub=0*S
2100      Set_smu(2)
2110      Force_v(Substrate,Vsub)
2120      !
2130      ! Define variables
2140      !
2150      N=0
2160      P=1
2170      Vgate_min(1)=.1*S
2180      Vgate_min(2)=.5*S
2190      Vgate_max(1)=.35*S
2200      Vgate_max(2)=5.0*S
2210      Vgate_step(1)=.1*S
2220      Vgate_step(2)=.5*S
2230      Ids_max=0..
2240      !
2250      Line=1
2260      Range=10.0*S
2270      Start(1)=.1*S
2280      Start(2)=.5*S
2290      Stop(1)=.3*S
2300      Stop(2)=5.0*S
2310      Number1=3
2320      Number2=10
2330      !
2340      Hold=1.0
2350      Dstep=.01
2360      Compl=.01*S
2370      !
2380      Current=2
2390      Irange=1.E-2*S
2400      !

```

! SET INTEGRATION TIME TO MEDIUM



```

2410 !
2420 ! Sweep Vds given Vgs THEN next Vgs
2430 !
2440 FOR Vgate=Vgate_min(P) TO Vgate_max(P) STEP Vgate_step(P)
2450     Force_v(Gate,Vgate)
2460     !
2470     Q=1
2480     Set_iv(Drain,Line,Range,Start(Q),Stop(Q),Number1,Hold,Dstep,Compl)
2490     Sweep_iv(Drain,Current,Irange,Id1(*),Vds1(*))
2500     Q=2
2510     Set_iv(Drain,Line,Range,Start(Q),Stop(Q),Number2,Hold,Dstep,Compl)
2520     Sweep_iv(Drain,Current,Irange,Id2(*),Vds2(*))
2530     !
2540     N=N+1
2550     T=0
2560     FOR T=1 TO 3
2570         Vds(T)=Vds1(T)
2580         Ids(T)=Id1(T)
2590         Id(N,T)=Ids(T)
2600         IF ABS(Id1(T))>ABS(Id1_max) THEN Id1_max=Id1(T)
2610     NEXT T
2620     FOR T=4 TO 13
2630         Vds(T)=Vds2(T-3)
2640         Ids(T)=Id2(T-3)
2650         Id(N,T)=Ids(T)
2660         IF ABS(Id2(T))>ABS(Id2_max) THEN Id2_max=Id2(T)
2670     NEXT T
2680     !
2690     !PRINT "N=";N;"Vgate=";Vgate
2700     !PRINT "Vds=";Vds1(*);Vds2(*)
2710     !PRINT "Ids=";Ids(*)
2720     Vgs(N)=Vgate
2730 NEXT Vgate
2740 !
2750 IF P=2 THEN GOTO 2790
2760 P=2
2770 GOTO 2440
2780 !
2790 ! Draw axes
2800 !
2810 Disable_port
2820 IF Ids_max=0. THEN Ids_max=100.
2830 CLEAR SCREEN
2840 IF S=-1 THEN GOTO 2870
2850 Lingraph1(0,6*S,0,Ids_max,"Vds","Ids","N-channel IV at Vbs=0V",1,1,"Vgs")
2860 GOTO 2890
2870 Lingraph1(0,6*S,0,Ids_max,"Vds","Ids","P-channel IV at Vbs=0V",1,1,"Vgs")
2880 !
2890 ! Plot an Id vs. Vd curve for a given Vg value
2900 !
2910 K=1
2920 FOR K=1 TO 13
2930     I=1
2940     FOR I=1 TO 13
2950         !PRINT "I=";I;"K=";K
2960         Ids(I)=Id(K,I)
2970     NEXT I
2980     !
2990     MOVE 0,0
3000     I=1

```

```

3010         FOR I=1 TO 13
3020             PLOT Vds(I),Ids(I)
3030         NEXT I
3040     NEXT K
3050     !
3060     PRINT " "
3070     PRINT "Width=",Width
3080     PRINT "Length=",Length
3090     PRINT "Type=",Type$
3100     PRINT " "
3110     PRINT Concat$
3120     PRINT " "
3130     PRINT " "
3140     PRINT " "
3150     PRINT " "
3160     PRINT " "
3170     PRINT " "
3180     PRINT " "
3190     PRINT " "
3200     !PRINT "Vds=";Vds(*)
3210     !PRINT "Vgs=";Vgs(*)
3220     !
3230     !*****
3240     !
3250     ! Data for KEYS in the following:
3260     !
3270     ! Vds(13)
3280     ! Vgs(13)
3290     ! Id(13,13)=Id(Vg,Vd).....Vg and Vd not defined
3300     ! Vsub
3310     !
3320     Disable_port
3330     !
3340     ! Write the data to the file
3350     !
3360     OUTPUT String_1$;"Vds   Vgs   Vbs   Ids"
3370     OUTPUT String_6$ USING "/,/,21A,/" ;String_1$
3380     OUTPUT @Path_1;String_6$
3390     I=1
3400     FOR I=1 TO 13
3410         K=1
3420         FOR K=1 TO 13
3430             OUTPUT String_2$ USING "SD.DDDE,/" ;Vds(K)
3440             OUTPUT @Path_1;String_2$
3450             !
3460             OUTPUT String_3$ USING "SD.DDDE,/" ;Vgs(I)
3470             OUTPUT @Path_1;String_3$
3480             !
3490             OUTPUT String_4$ USING "SD.DDDE,/" ;Vsub
3500             OUTPUT @Path_1;String_4$
3510             !
3520             OUTPUT String_5$ USING "SD.DDDE,/" ;Id(I,K)
3530             OUTPUT @Path_1;String_5$
3540         NEXT K
3550     NEXT I
3560     !
3570     ! Close the I/O path
3580     !
3590     ASSIGN @Path_1 TO *
3600     !

```

```
3610  !*****
3620  !
3630  GOSUB Debuginfo
3640!
3650  SUBEXIT
3660!
3670  Debuginfo: ! display input values
3680  PRINTER IS CRT
3690  !PRINT "algorithm <Keysiv_MOS>"
3700  !PRINT " W = ",W$
3710  !PRINT " R = ",R$
3720  !PRINT " C = ",C$
3730  RETURN
3740  SUBEND
3750  !
```

## APPENDIX D — Test Algorithm KEYSvt

```

10 !
20 ! APPENDIX D -- Test algorithm KEYSvt (the program used to obtain the Ids
30 ! versus Vgs curves on NIST8)
40 !
50 SUB Keysvt_mos(W$,R$,C$,INTEGER Pins(*),REAL Width,Length,Type$,Vbs(*),Vt(*)
60 Keysvt_mos: !*****
70 !*****
80 !
90 ! RE-STORE "/users/marshall/icms/ALG/BASIC/Keysvt_MOS"
100 !
110 ! LOADSUB ALL FROM "/usr/pcs/lib/XYGRAPH"
120 !
130 !*****
140 !
150 ! Programmers : Janet Marshall
160 !
170 ! Date : 04/17/1992 12:10:55
180 ! Revised : 04/17/1992 12:10:55
190 ! Device Class : MOSFET
200 ! Description : Mosfet drain current measurement at specified
210 ! : Vds,Vgs,Vbs and Vss.
220 ! Procedure :
230 !
240 ! Input Variables:
250 !
260 ! # Name Type Size Description
270 ! ---
280 ! Measurement Parameters:
290 ! 1 W S - Wafer Letter
300 ! 2 R S - Row Number
310 ! 3 C S - Column Number
320 !
330 ! Device Terminals:
340 ! 1 Gate I - Gate terminal
350 ! 2 Drain I - Drain terminal
360 ! 3 Source I - Source terminal
370 ! 4 Bulk I - Bulk terminal
380 ! 5 Sub I - Substrate contact
390 ! 6 Chuck I - Wafer chuck
400 !
410 ! Device Parameters:
420 ! 1 Width R - um, Mask channel width
430 ! 2 Length R - um, Mask channel length
440 ! 3 Type C - Channel type (P/N)
450 !
460 ! Output Variables:
470 !
480 ! # Name Type Size Description
490 ! ---
500 ! Output Parameters:
510 ! 1 Vbs A 4 Backgate bias
520 ! 2 Vt A 4 Threshold voltage
530 !
540 !*****
550 !
560 !
570 ! INPUT "Number of points in a sweep = ",Q
580 Q=50
590 OPTION BASE 1
600 !

```



```

610  INTEGER Gate,Drain,Source,Sub
620  INTEGER Line,I,J,K,M,N,P,Q,T,Current
630  INTEGER Number,M_max
640  REAL Vsub
650  !
660  ALLOCATE Ids(Q),Vgs(Q),Id(5,Q),Yn(5,Q)
670  DIM Yint(50),Ycalc(50),X(50),Y(50)
680  DIM File$(40),Dir$(40),Concat$(40)
690  DIM String_1$(40),String_2$(40),String_3$(40),String_4$(40)
700  !
710  !=====
720  !
730  ! Determine the filename
740  !
750  R$="0"
760  IF Length=2.0 THEN R$="1"
770  IF Length=3.0 AND (Width=6.0 OR Width=20.0) THEN R$="2"
780  IF Length=4.0 AND (Width=6.0 OR Width=20.0) THEN R$="3"
790  IF Length=5.0 AND (Width=6.0 OR Width=20.0) THEN R$="4"
800  IF Length=6.0 AND (Width=6.0 OR Width=20.0) THEN R$="5"
810  IF Length=8.0 AND (Width=6.0 OR Width=20.0) THEN R$="6"
820  !
830  IF Width=82. AND Type$="N" THEN R$="1"
840  IF Width=82. AND Type$="P" THEN R$="4"
850  IF Width=79. AND Type$="N" THEN R$="2"
860  IF Width=79. AND Type$="P" THEN R$="5"
870  IF Width=107. AND Type$="N" THEN R$="3"
880  IF Width=107. AND Type$="P" THEN R$="6"
890  !
900  IF Type$="P" THEN GOTO 1170
910  !
920  ! N-channel devices
930  !
940  IF Length=Width AND Length=3. THEN R$="1"
950  IF Length=Width AND Length=4. THEN R$="2"
960  IF Length=Width AND Length=5. THEN R$="3"
970  IF Length=Width AND Length=8. THEN R$="4"
980  IF Length=Width AND Length=10. THEN R$="5"
990  IF Length=Width AND Length=30. THEN R$="6"
1000 IF Length=Width AND Length=50. THEN R$="7"
1010 IF Length=Width AND Length=50. THEN C$="6"
1020 !
1030 IF R$="0" THEN R$="7"
1040 !
1050 IF R$="7" AND Width=3. THEN C$="1"
1060 IF R$="7" AND Width=4. THEN C$="2"
1070 IF R$="7" AND Width=5. THEN C$="4"
1080 IF R$="7" AND Width=8. THEN C$="5"
1090 IF R$="7" AND Width=10. THEN C$="7"
1100 IF R$="7" AND Length=10. THEN C$="8"
1110 IF R$="7" AND Width=30. THEN C$="10"
1120 IF R$="7" AND Length=30. THEN C$="11"
1130 GOTO 1390
1140 !
1150 ! P-channel devices
1160 !
1170 IF Length=Width AND Length=3. THEN R$="8"
1180 IF Length=Width AND Length=4. THEN R$="9"
1190 IF Length=Width AND Length=5. THEN R$="10"
1200 IF Length=Width AND Length=8. THEN R$="11"

```

```

1210 IF Length=Width AND Length=10. THEN R$="12"
1220 IF Length=Width AND Length=30. THEN R$="13"
1230 IF R$="10" THEN GOTO 1490
1240 !
1250 IF R$="0" THEN R$="10"
1260 !
1270 IF R$="10" AND Width=3. THEN C$="1"
1280 IF R$="10" AND Width=4. THEN C$="2"
1290 IF R$="10" AND Width=5. THEN C$="4"
1300 IF R$="10" AND Width=8. THEN C$="5"
1310 IF R$="10" AND Width=10. THEN C$="7"
1320 IF R$="10" AND Length=10. THEN C$="8"
1330 IF R$="10" AND Width=30. THEN C$="10"
1340 IF R$="10" AND Length=30. THEN C$="11"
1350 GOTO 1490
1360 !
1370 ! Chip OOM
1380 !
1390 IF C$<>"0" THEN GOTO 1490
1400 IF Width=120 OR Width=1760 THEN R$="12"
1410 IF Width=80 OR Width=1320 THEN R$="13"
1420 IF Width>1000 THEN C$="9"
1430 !
1440 IF Pins(2)=18 OR Pins(1)=8 THEN C$="7"
1450 IF Pins(2)=46 OR Pins(2)=48 THEN C$="11"
1460 !
1470 !=====
1480 !
1490 Dir$="/users/marshall/nist8data/"
1500 !
1510 File$="W"&W$&"R"&R$&"C"&C$&"VB.DAT"
1520 !
1530 Concat$=Dir$&File$
1540 !
1550 !PRINT Concat$
1560 !
1570 !-----
1580 !
1590 ! Specify default mass storage
1600 !
1610 !MASS STORAGE IS ":",600,1"
1620 !
1630 ! Create ASCII data file with 10 sectors on the specified
1640 !      mass storage device (:,600,1)
1650 !
1660 ON ERROR GOTO File_exists
1670 CREATE ASCII Concat$,10
1680 File_exists:      OFF ERROR
1690 !
1700 ! Assign (or open) an I/O path name to the file
1710 !
1720 ASSIGN @Path_1 TO Concat$
1730 !
1740 !-----
1750 !
1760 Init_system
1770 !
1780 ! Define measurement pins
1790 !
1800 Gate=Pins(1)

```

```

1810 Drain=Pins(2)
1820 Source=Pins(3)
1830 Sub=Pins(4)
1840 !
1850 ! Connect pins to sources
1860 !
1870 Connect(FNSmu(1),Drain)
1880 Connect(FNSmu(2),Gate)
1890 Connect(FNGnd,Source)
1900 Connect(FNSmu(3),Sub)
1910 !
1920 ! Force bias conditions
1930 !
1940 IF Type$="N" THEN S=1.0
1950 IF Type$="P" THEN S=-1.0
1960 !
1970 Vds=.2*S
1980 Set_smu(2) ! SET INTEGRATION TIME TO MEDIUM
1990 Force_v(Drain,Vds)
2000 !
2010 ! Define variables
2020 !
2030 P=0
2040 Vbs_min=0.*S
2050 Vbs_max=-9.0*S
2060 Vbs_step=-3.0*S
2070 Ids_max=0.
2080 !
2090 Line=1
2100 Vrange=10.0*S
2110 Start=.1*S
2120 Stop=5.0*S
2130 Number=50
2140 !
2150 Hold=1.0
2160 Dstep=.01
2170 Icompl=.01*S
2180 !
2190 Current=2
2200 Irange=.01*S
2210 !
2220 PRINT " "
2230 PRINT " "
2240 !
2250 ! Sweep Vgs given Vbs THEN next Vbs
2260 !
2270 FOR Vsub=Vbs_min TO Vbs_max STEP Vbs_step
2280 Force_v(Sub,Vsub)
2290 !
2300 Set_iv(Gate,Line,Vrange,Start,Stop,Number,Hold,Dstep,Icompl)
2310 Sweep_iv(Drain,Current,Irange,Ids(*),Vgs(*))
2320 !
2330 P=P+1
2340 !PRINT "P=";P;"Vbs=";Vsub
2350 !PRINT "Vgs=";Vgs(*)
2360 !PRINT "Ids=";Ids(*)
2370 Vbs(P)=Vsub
2380 I=1
2390 FOR I=1 TO 50
2400 Yn(P,I)=Ids(I)

```

```

2410         Id(P,I)=Ids(I)
2420         IF ABS(Ids(I))>ABS(Ids_max) THEN Ids_max=Ids(I)
2430     NEXT I
2440     !
2450 NEXT Vsub
2460 !
2470 Disable_port
2480 !
2490 ! Draw axes
2500 !
2510 CLEAR SCREEN
2520 IF Ids_max=0. THEN Ids_max=100.
2530 IF S=-1 THEN GOTO 2560
2540 Lingraph1(0,6*S,0,Ids_max,"Vgs","Ids","N-channel Vt at Vds=.2V",1,1,"Vbs"
2550 GOTO 2580
2560 Lingraph1(0,6*S,0,Ids_max,"Vgs","Ids","P-channel Vt at Vds=-.2V",1,1,"Vbs
2570 !
2580 ! Plot an Id vs. Vg curve for a given Vbs value
2590 !
2600 K=1
2610 FOR K=1 TO 4
2620     I=1
2630     FOR I=1 TO Q
2640         Ids(I)=Yn(K,I)
2650     NEXT I
2660     !
2670     MOVE 0,0
2680     I=1
2690     FOR I=1 TO Q
2700         !PRINT "K=";K;"I=";I;"Q=";Q
2710         PLOT Vgs(I),Ids(I)
2720     NEXT I
2730 NEXT K
2740 !
2750 PRINT " "
2760 PRINT "Width=",Width
2770 PRINT "Length=",Length
2780 PRINT "Type=",Type$
2790 PRINT " "
2800 PRINT Concat$
2810 PRINT " "
2820 !PRINT "Vgs=";Vgs(*)
2830 !PRINT "Vbs=";Vbs(*)
2840 !PRINT "Ids=";Ids(*)
2850 !
2860 ! Data for Id vs. Vg curves in the following:
2870 !
2880 ! Vds
2890 ! Vgs(50)
2900 ! Id(5,50)=Id(Vbs,Vg).....Vbs and Vg not defined
2910 ! Vbs(4)
2920 !
2930 !*****
2940 !
2950 ! Find Vt for the different values of Vbs
2960 !
2970 T=0
2980 Vsub=Vbs_min
2990 FOR Vsub=Vbs_min TO Vbs_max STEP Vbs_step
3000     !

```



```

3010      ! Sweep the Id vs. Vg curve
3020      !
3030      T=T+1
3040      I=1
3050      FOR I=1 TO Q
3060          X(I)=Vgs(I)
3070          Y(I)=Yn(T,I)
3080      NEXT I
3090      !
3100      Slope_max=1.E-11
3110      Rms_max=0.
3120      Xint_max=0.
3130      M_max=0
3140      N=5
3150      M=1
3160      FOR M=1 TO 45
3170          !
3180          GOTO Lnfit
3190          !
3200      Back:      Z=0
3210                  IF ABS(Slope)>ABS(Slope_max) THEN M_max=M
3220                  !PRINT "Slope=";Slope;"Slope_max=";Slope_max;"M_max=";M_max;"M=";
3230                  IF ABS(Slope)>ABS(Slope_max) THEN Xint_max=Xint
3240                  IF ABS(Slope)>ABS(Slope_max) THEN Rms_max=Rms
3250                  IF ABS(Slope)>ABS(Slope_max) THEN Slope_max=Slope
3260                  !PRINT "Xint=",Xint;"M=";M
3270                  !
3280          NEXT M
3290          !
3300          Vt(T)=Xint_max-.5*Vds
3310          PRINT "Vbs=";Vsub;"Vt=";Vt(T);"M_max=";M_max
3320          !
3330      NEXT Vsub
3340      PRINT " "
3350      PRINT " "
3360      PRINT " "
3370      GOTO Stop
3380      !
3390      !*****
3400      !
3410      ! Subroutine LNFIT (N,M,X,Y,Slope,Xint,Rms)
3420      !
3430      ! N = # points
3440      ! M = start value of dimension
3450      !
3460      !DIM X(1),Y(1)
3470      !DIM Yint(101),Ycalc(101)
3480      !
3490      Lnfit:      I=0
3500      Sumx=0
3510      Sumy=0
3520      Sumxy=0
3530      Sumxx=0
3540      !
3550      FOR I=M TO M+N-1
3560          !PRINT "X=";X(I);"Y=";Y(I)
3570          Sumx=Sumx+X(I)
3580          Sumy=Sumy+Y(I)
3590          Sumxy=Sumxy+X(I)*Y(I)
3600          Sumxx=Sumxx+X(I)*X(I)

```

```

3610 NEXT I
3620 !
3630 Anums=N*Sumxy-Sumx*Sumy
3640 !PRINT "Anums=";Anums
3650 Anumi=Sumxx*Sumy-Sumx*Sumxy
3660 !PRINT "Anumi=";Anumi
3670 Den=N*Sumxx-Sumx*Sumx
3680 !PRINT "Den=";Den
3690 IF Den=0 THEN GOTO 3780
3700 Slope=Anums/Den
3710 !PRINT "Slope=";Slope
3720 Yint(M)=Anumi/Den
3730 IF Anums=0. THEN Xint=999
3740 IF Anums=0. THEN GOTO 3780
3750 Xint=-Anumi/Anums
3760 !PRINT "Xint=";Xint
3770 !
3780 ! Determine the RMS deviation in the Y direction
3790 !
3800 J=0
3810 Squ=0
3820 FOR J=M TO M+N-1
3830     Ycalc(J)=Slope*X(J)+Yint(M)
3840     Squ=Squ+(Y(J)-Ycalc(J))^2
3850 NEXT J
3860 !
3870 Rms=SQR(Squ/N)
3880 !
3890 GOTO Back
3900 !*****
3910 !
3920 ! Data for KEYS in the following
3930 !
3940 ! Vbs(4)
3950 ! Vt(4)
3960 !
3970 Stop:  Disable_port
3980 !
3990 ! Write data to the file
4000 !
4010 OUTPUT String_4$;"Vbs then Vt values"
4020 OUTPUT String_1$ USING "//,18A,/" ;String_4$
4030 OUTPUT @Path_1;String_1$
4040 K=1
4050 FOR K=1 TO 4
4060     OUTPUT String_2$ USING "DDD.DDD,/" ;Vbs(K)
4070     OUTPUT @Path_1;String_2$
4080     !
4090     OUTPUT String_3$ USING "DDD.DDD,/" ;Vt(K)
4100     OUTPUT @Path_1;String_3$
4110 NEXT K
4120 !
4130 ! Close the I/O path
4140 !
4150 ASSIGN @Path_1 TO *
4160 !
4170 !*****
4180 !
4190 GOSUB Debuginfo
4200!

```

```
4210 SUBEXIT
4220!
4230 Debuginfo: ! display input values
4240 PRINTER IS CRT
4250 !PRINT "algorithm <Keysvt_MOS>"
4260 !PRINT " W = ",W$
4270 !PRINT " R = ",R$
4280 !PRINT " C = ",C$
4290 RETURN
4300 SUBEND
4310 !
```

## APPENDIX E — Test Algorithm INV

```

10 !
20 ! APPENDIX E -- Test algorithm INV (the program used to obtain the Vin
30 !          versus Vout curves on NIST8)
40 !
50 SUB Inv_inv(W$,R$,C$,INTEGER Pins(*),REAL Nwidth,Nlength,Pwidth,Plength,Vou
60 Inv_inv: !*****
70 !
80 ! RE-STORE "/users/marshall/icms/ALG/BASIC/Inv_INV"
90 !
100 ! LOADSUB ALL FROM "/usr/pcs/lib/XYGRAPH"
110 !
120 ! *****
130 !
140! Programmers : Janet Marshall
150!
160! Date : 04/21/1992 12:22:10
170! Revised : 04/21/1992 12:22:10
180! Device Class : INVERTER
190! Description : Mosfet drain current measurement at specified
200! : Vds,Vgs,Vbs and Vss.
210! Procedure :
220!
230! Input Variables:
240!
250! # Name Type Size Description
260! ---
270! Measurement Parameters:
280! 1 W S - Wafer Letter
290! 2 R S - Row Number
300! 3 C S - Column Number
310!
320! Device Terminals:
330! 1 VCC I - Vcc terminal
340! 2 VSS I - Vss terminal
350! 3 NW I - N-well terminal
360! 4 PW I - P-well terminal
370! 5 IN I - Data input
380! 6 OUT I - Data output
390! 7 Chuck I - Wafer chuck
400!
410! Device Parameters:
420! 1 NWidth R - um, Mask n-channel width
430! 2 NLength R - um, Mask n-channel length
440! 3 PWidth R - um, Mask p-channel width
450! 4 PLength R - um, Mask p-channel length
460!
470! Output Variables:
480!
490! # Name Type Size Description
500! ---
510! Output Parameters:
520! 1 Vout A 51 Output Voltage
530! 2 Vin A 51 Input Voltage
540!
550! *****
560!
570 OPTION BASE 1
580 !
590 INTEGER Vcc,Vss,Nwell,Pwell,In,Out
600 INTEGER I,J,M,N,Q

```



```

610     INTEGER Line,Voltage,Number
620     Q=51
630     !
640     ALLOCATE X(Q),Y(Q),Yint(Q),Ycalc(Q)
650     DIM File$(40),Dir$(40),Concat$(40)
660     DIM String_1$(40),String_2$(40),String_3$(40),String_4$(40)
670     !
680     !=====
690     !
700     ! Determine the filename
710     !
720     !C$="9"
730     !
740     IF Nlength=3.0 THEN R$="1"
750     IF Nlength=4.0 THEN R$="3"
760     IF Nlength=6.0 THEN R$="4"
770     IF Nlength=10.0 THEN R$="6"
780     !
790     Dir$="/users/marshall/data/"
800     !
810     File$="W"&W$&"R"&R$&"C"&C$&"IV.DAT"
820     !
830     Concat$=Dir$&File$
840     !
850     !PRINT Concat$
860     !
870     ! Create ASCII data file with 10 sectors
880     !
890     ON ERROR GOTO File_exists
900     CREATE ASCII Concat$,10
910 File_exists:      OFF ERROR
920     !
930     ! Assign (or open) an I/O path name to the file
940     !
950     ASSIGN @Path_1 TO Concat$
960     !
970     !=====
980     !
990     Init_system
1000    !
1010    ! Define measurement pins
1020    !
1030    Vcc=Pins(1)
1040    Vss=Pins(2)
1050    Nwell=Pins(3)
1060    Pwell=Pins(4)
1070    In=Pins(5)
1080    Out=Pins(6)
1090    !
1100    ! Connect pins to sources
1110    !
1120    Connect(FNSmu(3),Vcc)
1130    Connect(FNGnd,Vss)
1140    Connect(FNSmu(3),Nwell)
1150    Connect(FNGnd,Pwell)
1160    Connect(FNSmu(2),In)
1170    Connect(FNSmu(1),Out)
1180    !
1190    ! Force bias conditions
1200    !

```

```

1210 Vdd=5.0
1220 Set_smu(2) ! SET INTEGRATION TIME TO MEDIUM
1230 Force_v(Vcc,Vdd)
1240 Force_v(Nwell,Vdd)
1250 !
1260 ! Define variables
1270 !
1280 Line=1
1290 Range=10.0
1300 Start=0.
1310 Stop=5.0
1320 Number=51
1330 !
1340 Hold=1.0
1350 Dstep=.01
1360 Icompl=.01
1370 !
1380 Voltage=1
1390 Vrange=10.0
1400 !
1410 ! Sweep Vin to get Vout
1420 !
1430 Set_iv(In,Line,Range,Start,Stop,Number,Hold,Dstep,Icompl)
1440 Sweep_iv(Out,Voltage,Vrange,Vout(*),Vin(*))
1450 !
1460 ! Draw axes
1470 !
1480 Disable_port
1490 CLEAR SCREEN
1500 PRINT " "
1510 !
1520 Lingraph1(0,6,0,6,"Vin","Vout","Vout vs. Vin",1,1)
1530 !
1540 ! Plot an Id vs. Vg curve for a given Vbs value
1550 !
1560 MOVE 0,0
1570 FOR I=1 TO Q
1580     PLOT Vin(I),Vout(I)
1590     X(I)=Vin(I)
1600     Y(I)=Vout(I)
1610     !PRINT "Vin=";Vin(I);"Vout=";Vout(I)
1620 NEXT I
1630 !
1640 ! Data for Vout vs. Vin curves in the following:
1650 !
1660 ! Vin(51)
1670 ! Vout(51)
1680 !
1690 !*****
1700 !
1710 ! Find the values of Vout and Vin where the maximum slope exists
1720 !
1730 !
1740 ! Sweep the Vout vs. Vin curve
1750 !
1760 N=5
1770 FOR M=1 TO 47
1780     !
1790     GOTO Lnfit
1800     !

```

```

1810 Back: IF ABS(Slope)>ABS(Slope_max) THEN M_max=M
1820       IF ABS(Slope)>ABS(Slope_max) THEN Slope_max=Slope
1830       !
1840     NEXT M
1850     !
1860     PRINT "Vin=";X(M_max+2);"Vout=";Y(M_max+2);"Slope_max=";Slope_max
1870     PRINT " "
1880     PRINT Concat$
1890     PRINT " "
1900     PRINT " "
1910     PRINT " "
1920     PRINT " "
1930     PRINT " "
1940     PRINT " "
1950     PRINT " "
1960     PRINT " "
1970     PRINT " "
1980     PRINT " "
1990     PRINT " "
2000     !
2010     GOTO Stop
2020     !
2030     !*****
2040     !
2050     ! Subroutine LNFIT (N,M,X,Y,Slope,Xint,Rms)
2060     !
2070     ! N = # points
2080     ! M = start value of dimension
2090     !
2100     !DIM X(1),Y(1)
2110     !DIM Yint(101),Ycalc(101)
2120     !
2130   Lnfit: I=0
2140     Sumx=0
2150     Sumy=0
2160     Sumxy=0
2170     Sumxx=0
2180     !
2190     FOR I=M TO M+N-1
2200       !PRINT "X=";X(I);"Y=";Y(I)
2210       Sumx=Sumx+X(I)
2220       Sumy=Sumy+Y(I)
2230       Sumxy=Sumxy+X(I)*Y(I)
2240       Sumxx=Sumxx+X(I)*X(I)
2250     NEXT I
2260     !
2270     Anums=N*Sumxy-Sumx*Sumy
2280     !PRINT "Anums=";Anums
2290     Anumi=Sumxx*Sumy-Sumx*Sumxy
2300     !PRINT "Anumi=";Anumi
2310     Den=N*Sumxx-Sumx*Sumx
2320     !PRINT "Den=";Den
2330     IF Den=0 THEN GOTO 2410
2340     Slope=Anums/Den
2350     !PRINT "Slope=";Slope
2360     Yint(M)=Anumi/Den
2370     IF Anums=0. THEN Xint=999
2380     IF Anums=0. THEN GOTO 2410
2390     Xint=-Anumi/Anums
2400     !

```

```

2410 ! Determine the RMS deviation in the Y direction
2420 !
2430 J=0
2440 Squ=0
2450 FOR J=M TO M+N-1
2460     Ycalc(J)=Slope*X(J)+Yint(M)
2470     Squ=Squ+(Y(J)-Ycalc(J))^2
2480 NEXT J
2490 !
2500 Rms=SQRT(Squ/N)
2510 !
2520 GOTO Back
2530 !*****
2540 !
2550 Stop:  Disable_port
2560 !
2570 ! Write the data to the file
2580 !
2590 OUTPUT String_1$;"Vin Vout"
2600 OUTPUT String_2$ USING "//,8A,/" ;String_1$
2610 OUTPUT @Path_1;String_2$
2620 I=1
2630 FOR I=1 TO 51
2640     OUTPUT String_3$ USING "SD.DDD,/" ;Vin(I)
2650     OUTPUT @Path_1;String_3$
2660     !
2670     OUTPUT String_4$ USING "SD.DDD,/" ;Vout(I)
2680     OUTPUT @Path_1;String_4$
2690 NEXT I
2700 !
2710 ! Close the I/O path
2720 !
2730 ASSIGN @Path_1 TO *
2740 !
2750 !*****
2760 !
2770 GOSUB Debuginfo
2780 !
2790 SUBEXIT
2800 !
2810 Debuginfo: ! display input values
2820 PRINTER IS CRT
2830 !PRINT "algorithm <INV_MOS>"
2840 !PRINT " W = ",W$
2850 !PRINT " R = ",R$
2860 !PRINT " C = ",C$
2870 RETURN
2880 SUBEND
2890 !

```



## APPENDIX F — Test Algorithm SRAM

```

10 !
20 ! APPENDIX F -- Test algorithm SRAM (the program used to determine the
30 ! functionality of the static RAM on NIST8)
40 !
50 SUB Sram_sra(W$,R$,C$,INTEGER Pins(*),REAL Nwidth,Nlength,Pwidth,Plength)
60 Sram_sra: !*****
70 !
80 ! RE-STORE "/users/marshall/icms/ALG/BASIC/Sram_SRA"
90 !
100 ! LOADSUB ALL FROM "/usr/pcs/lib/XYGRAPH"
110 !
120 !*****
130 !
140 ! Programmers : Janet Marshall
150 !
160 ! Date : 04/21/1992 13:19:17
170 ! Revised : 04/21/1992 13:19:17
180 ! Device Class : SRAM
190 ! Description : Mosfet drain current measurement at specified
200 ! : Vds,Vgs,Vbs and Vss.
210 ! Procedure :
220 !
230 ! Input Variables:
240 !
250 ! # Name Type Size Description
260 ! ---
270 ! Measurement Parameters:
280 ! 1 W S - Wafer Letter
290 ! 2 R S - Row Number
300 ! 3 C S - Column Number
310 !
320 ! Device Terminals:
330 ! 1 VCC I - Vcc terminal
340 ! 2 VSS I - Vss terminal
350 ! 3 NW I - N-well terminal
360 ! 4 PW I - P-well terminal
370 ! 5 WSEL I - Write select
380 ! 6 RWSEL I - Read-write select
390 ! 7 LAT I - Data latch
400 ! 8 BIT I - Bit
410 ! 9 BITBAR I - Bitbar
420 ! 10 DATA I - Data
430 ! 11 DATAB I - Databar
440 ! 12 CHUCK I - Wafer chuck
450 !
460 ! Device Parameters:
470 ! 1 NWidth R - um, Mask n-channel width
480 ! 2 NLength R - um, Mask n-channel length
490 ! 3 PWidth R - um, Mask p-channel width
500 ! 4 PLength R - um, Mask p-channel length
510 !
520 ! Output Variables:
530 !
540 ! # Name Type Size Description
550 ! ---
560 ! Output Parameters:
570 ! none
580 !
590 !*****
600 !

```

```

610     OPTION BASE 1
620     !
630     INTEGER Rwsel,Vcc,Nwell,Latch,Pwell,Bitbar,Databar,Bit,Data,Vss,Wsel
640     INTEGER I,J,M,N,Q
650     Q=13
660     !
670     ALLOCATE Datao(Q),Databaro(Q),Ind(Q+1)
680     ALLOCATE Biti(Q),Bitbari(Q),Rw(Q),W(Q),Lat(Q)
690     DIM File$(40),Dir$(40),Concat$(40)
700     DIM String_1$(40),String_2$(40),String_3$(40),String_4$(40)
710     !
720     !=====
730     !
740     ! Determine the filename
750     !
760     Dir$="/users/marshall/data/"
770     !
780     File$="W"&W$&"R"&R$&"C"&C$&"SR.DAT"
790     !
800     Concat$=Dir$&File$
810     !
820     ! Create an ASCII data file with 10 sectors
830     !
840     ON ERROR GOTO File_exists
850     CREATE ASCII Concat$,10
860 File_exists:          OFF ERROR
870     !
880     ! Assign (or open) and I/O path name to the file
890     !
900     ASSIGN @Path_1 TO Concat$
910     !
920     !=====
930     !
940     Init_system
950     !
960     ! Define measurement pins
970     !
980     Rwsel=Pins(6)
990     Vcc=Pins(1)
1000    Nwell=Pins(3)
1010    Latch=Pins(7)
1020    Pwell=Pins(4)
1030    Bitbar=Pins(9)
1040    Databar=Pins(11)
1050    Bit=Pins(8)
1060    Data=Pins(10)
1070    Vss=Pins(2)
1080    Wsel=Pins(5)
1090    !
1100    ! Connect pins to sources
1110    !
1120    Connect(FNSmu(1),Data)
1130    Connect(FNSmu(2),Latch)
1140    Connect(FNSmu(3),Rwsel)
1150    Connect(FNSmu(4),Databar)
1160    !
1170    Connect(FNAux(1),Wsel)
1180    !
1190    Connect(FNAux(2),Vcc)
1200    Connect(FNAux(2),Nwell)

```

```

1210 Connect(FNAux(2),Bit)
1220 !
1230 Connect(FNGnd,Vss)
1240 Connect(FNGnd,Pwell)
1250 Connect(FNGnd,Bitbar)
1260 !
1270 ! Force the INITIAL bias conditions
1280 !
1290 Vgnd=0.
1300 Vdd=5.0
1310 Value=Vdd
1320 Valuebar=Vgnd
1330 I=0
1340 J=1
1350 Ind(J)=J
1360 !
1370 Force_v(Vcc,Vdd)
1380 Force_v(Nwell,Vdd)
1390 Force_v(Bit,Value)
1400 !
1410 Force_v(Latch,Vgnd)
1420 Force_v(Rwsel,Vgnd)
1430 Force_v(Wsel,Vgnd)
1440 !
1450 Measure_v(Data,Datao(J))
1460 Measure_v(Databar,Databaro(J),0)
1470 !
1480 PRINT "I";J
1490 !PRINT "Dataout=";Datao(J);"Databarout=";Databaro(J)
1500 !PRINT "Dataout=";Datao(J)
1510 Biti(J)=Value
1520 Bitbari(J)=Valuebar
1530 Rw(J)=0.
1540 W(J)=0.
1550 Lat(J)=0.
1560 J=J+1
1570 Ind(J)=J
1580 !
1590 ! Perform a WRITE
1600 !
1610 PRINT " "
1620 I=I+1
1630 Force_v(Latch,Vdd)
1640 Force_v(Rwsel,Vdd)
1650 Force_v(Wsel,Vdd)
1660 WAIT 1
1670 Force_v(Latch,Vgnd)
1680 Force_v(Rwsel,Vgnd)
1690 Force_v(Wsel,Vgnd)
1700 !
1710 Measure_v(Data,Datao(J))
1720 Measure_v(Databar,Databaro(J))
1730 PRINT "W";J
1740 !PRINT "Dataout=";Datao(J);"Databarout=";Databaro(J)
1750 !PRINT "Dataout=";Datao(J)
1760 Biti(J)=Value
1770 Bitbari(J)=Valuebar
1780 Rw(J)=5.
1790 W(J)=5.
1800 Lat(J)=5.

```

```

1810 J=J+1
1820 Ind(J)=J
1830 !
1840 ! Change the Datain
1850 !
1860 IF I=2 OR I=4 THEN GOTO 2080
1870 Connect(FNSmu(6),Bitbar)
1880 Connect(FNGnd,Bit)
1890 Value=0.
1900 Valuebar=5.0
1910 Force_v(Bitbar,Valuebar)
1920 Execute
1930 !
1940 Measure_v(Data,Datao(J))
1950 Measure_v(Databar,Databaro(J))
1960 PRINT "D";J
1970 !PRINT "Dataout=";Datao(J);"Databarout=";Databaro(J)
1980 !PRINT "Dataout=";Datao(J)
1990 Biti(J)=Value
2000 Bitbari(J)=Valuebar
2010 Rw(J)=0.
2020 W(J)=0.
2030 Lat(J)=0.
2040 J=J+1
2050 Ind(J)=J
2060 GOTO 2300
2070 !
2080 ! Rechange the Datain
2090 !
2100 Connect(FNSmu(6),Bit)
2110 Connect(FNGnd,Bitbar)
2120 Value=5.0
2130 Valuebar=0.
2140 Force_v(Bit,Value)
2150 Execute
2160 !
2170 Measure_v(Data,Datao(J))
2180 Measure_v(Databar,Databaro(J))
2190 PRINT "D";J
2200 !PRINT "Dataout=";Datao(J);"Databarout=";Databaro(J)
2210 !PRINT "Dataout=";Datao(J)
2220 Biti(J)=Value
2230 Bitbari(J)=Valuebar
2240 Rw(J)=0.
2250 W(J)=0.
2260 Lat(J)=0.
2270 J=J+1
2280 Ind(J)=J
2290 !
2300 ! Perform a READ
2310 !
2320 WAIT 1
2330 Force_v(Rwsel,Vdd)
2340 Force_v(Wsel,Vgnd)
2350 Force_v(Latch,Vgnd)
2360 !
2370 Measure_v(Data,Datao(J))
2380 Measure_v(Databar,Databaro(J))
2390 PRINT "R";J;"*"
2400 !PRINT "Dataout=";Datao(J);"Databarout=";Databaro(J)

```



```

2410      !PRINT "Dataout=";Datao(J)
2420      Biti(J)=Value
2430      Bitbari(J)=Valuebar
2440      Rw(J)=5.
2450      W(J)=0.
2460      Lat(J)=0.
2470      J=J+1
2480      Ind(J)=J
2490      !
2500      Force_v(Rwsel,Vgnd)
2510      IF I=4 THEN GOTO 2540
2520      GOTO 1590
2530      !
2540      ! Draw axes
2550      !
2560      Disable_port
2570      CLEAR SCREEN
2580      !
2590      Lingraph1(0,Q+1,0,6,"Time","Datain","Datain vs. Time",1,1,"SRAM")
2600      !
2610      ! Plot Datain vs. Time
2620      !
2630      MOVE 0,0
2640      M=1
2650      FOR M=1 TO Q
2660          PLOT Ind(M),Biti(M)
2670          !PRINT "Ind";Ind(M);"Datain=";Biti(M)
2680      NEXT M
2690      !
2700      ! Draw axes
2710      !
2720      Lingraph1(0,Q+1,0,6,"Time","Dataout","Dataout vs. Time",1,4,"SRAM")
2730      !
2740      ! Plot Data vs. Time
2750      !
2760      MOVE 0,0
2770      M=1
2780      FOR M=1 TO Q
2790          PLOT Ind(M),Datao(M)
2800          !PRINT "Ind";Ind(M);"Data=";Datao(M)
2810      NEXT M
2820      !
2830      ! Draw axes
2840      !
2850      Lingraph1(0,Q+1,0,6,"Time","Rwsel","Rwsel vs. Time",1,3,"SRAM")
2860      !
2870      ! Plot Rwsel, Wsel, or Latch vs. Time
2880      !           Rw(J), W(J),      Lat(J)
2890      !
2900      MOVE 0,0
2910      M=1
2920      FOR M=1 TO Q
2930          PLOT Ind(M),Rw(M)
2940          !PRINT "Ind";Ind(M);"Rwsel=";Rw(M)
2950      NEXT M
2960      !
2970      ! Draw axes
2980      !
2990      Lingraph1(0,Q+1,0,6,"Time","Databarout","Databarout vs. Time",1,2,"SRAM")
3000      !

```

```

3010 ! Plot Databarout vs. Time
3020 !
3030 MOVE 0,0
3040 M=1
3050 FOR M=1 TO Q
3060     PLOT Ind(M),Databaro(M)
3070     !PRINT "Ind";Ind(M);"Databaro=";Databaro(M)
3080 NEXT M
3090 !
3100 ! Data for Datao vs. Time curves in the following:
3110 !
3120 ! Datao(5)
3130 ! Databaro(5)
3140 ! Time(5)
3150 !
3160 !*****
3170 !
3180 Disable_port
3190 PRINT Concat$
3200 !
3210 ! Write the data to the file
3220 !
3230 OUTPUT String_1$;"SRAM Data"
3240 OUTPUT String_2$ USING "//,15A,/" ;String_1$
3250 OUTPUT @Path_1;String_2$
3260 !
3270 ! Close the I/O path
3280 !
3290 ASSIGN @Path_1 TO *
3300 !
3310 !*****
3320 !
3330 GOSUB Debuginfo
3340 !
3350 SUBEXIT
3360 !
3370 Debuginfo: ! display input values
3380 PRINTER IS CRT
3390 !PRINT "algorithm <Sram_SRA>"
3400 !PRINT " W = ",W$
3410 !PRINT " R = ",R$
3420 !PRINT " C = ",C$
3430 RETURN
3440 SUBEND
3450 !

```

# APPENDIX G — SPICE File for an N-Channel MOSFET

```

*
* Appendix G - SPICE file (named ivcharn.cel) for an n-channel MOSFET
*
* filename = [marshall.simox]nist8mod.fil
*
* FILENAME = NMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODN NMOS LEVEL=2 LD=0.250000U TOX=413.000008E-10
+ NSUB=6.294117E+15 VT0=0.807671 KP=4.465000E-05 GAMMA=0.5467
+ PHI=0.6 U0=534.071 UEXP=.16209 UCRIT=90795.9
+ DELTA=1.01989 VMAX=57490.9 XJ=0.250000U LAMBDA=3.494828E-02
+ NFS=5.034625E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=28.380000 CGD0=3.135421E-10 CGS0=3.135421E-10 CGB0=3.907717E-10
+ CJ=9.308500E-05 MJ=0.693518 CJSW=5.398300E-10 MJSW=0.284549 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.28 um
*
* FILENAME = PMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODP PMOS LEVEL=2 LD=0.152257U TOX=413.000008E-10
+ NSUB=7.140277E+15 VT0=-0.807327 KP=2.383000E-05 GAMMA=0.5823
+ PHI=0.6 U0=284.969 UEXP=0.231562 UCRIT=15586.3
+ DELTA=0.920741 VMAX=45761.7 XJ=0.250000U LAMBDA=5.083543E-02
+ NFS=7.553318E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=87.650000 CGD0=1.909559E-10 CGS0=1.909559E-10 CGB0=3.770536E-10
+ CJ=2.500000E-04 MJ=0.545647 CJSW=3.174900E-10 MJSW=0.330136 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.20 um
*
*
*
* FILENAME = IVCHARN.FIL
* NOTE: Use with MODEL.FIL to make IVCHARN.CEL
*
* N-CHANNEL MOS OUTPUT CHARACTERISTICS
*
M1 1 2 0 0 MODN L=3.0UM W=6.0UM AD=12.5P AS=12.5P PD=15U
+ PS=15U NRD=2.0 NRS=2.0
*
VD 3 0
VG 2 0
VIDS 3 1
*
.OPTIONS NODE NOPAGE
.DC VD 0 5 .5 VG 0 5 1
.PLOT DC I(VIDS)
.END

```

# APPENDIX H — SPICE File for an Inverter

```

*
* Appendix H - SPICE file (named inverter.cel) for an inverter
*
* filename = [marshall.simox]nist8mod.fil
*
* FILENAME = NMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODN NMOS LEVEL=2 LD=0.250000U TOX=413.000008E-10
+ NSUB=6.294117E+15 VT0=0.807671 KP=4.465000E-05 GAMMA=0.5467
+ PHI=0.6 U0=534.071 UEXP=.16209 UCRIT=90795.9
+ DELTA=1.01989 VMAX=57490.9 XJ=0.250000U LAMBDA=3.494828E-02
+ NFS=5.034625E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=28.380000 CGD0=3.135421E-10 CGS0=3.135421E-10 CGB0=3.907717E-10
+ CJ=9.308500E-05 MJ=0.693518 CJSW=5.398300E-10 MJSW=0.284549 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.28 um
*
* FILENAME = PMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODP PMOS LEVEL=2 LD=0.152257U TOX=413.000008E-10
+ NSUB=7.140277E+15 VT0=-0.807327 KP=2.383000E-05 GAMMA=0.5823
+ PHI=0.6 U0=284.969 UEXP=0.231562 UCRIT=15586.3
+ DELTA=0.920741 VMAX=45761.7 XJ=0.250000U LAMBDA=5.083543E-02
+ NFS=7.553318E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=87.650000 CGD0=1.909559E-10 CGS0=1.909559E-10 CGB0=3.770536E-10
+ CJ=2.500000E-04 MJ=0.545647 CJSW=3.174900E-10 MJSW=0.330136 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.20 um
*
*
*
* FILENAME = INVERTER.FIL
*
.SUBCKT INVERT 1 2 3
*
M1 100 1 0 0 MODN L=3.00UM W=6.00UM AD=84P AS=84P PD=40U
+ PS=40U NRD=2.0 NRS=2.0
M2 100 1 3 3 MODP L=3.00UM W=12.0UM AD=144P AS=144P PD=48U
+ PS=48U NRD=1.0 NRS=1.0
R1 100 2 300
C1 2 0 50P
*
.ENDS INVERT
*
*
X1 1 2 3 INVERT
*
VIN 1 0
VCC 3 0 5V
*
.OPTIONS LIMPTS=500

```



```
.DC VIN 0.5 4.5 0.1  
.PLOT DC V(2)  
.END
```

# APPENDIX I — SPICE File for a Ring Oscillator

```

*
* Appendix I - SPICE file (named ring.cel) for a ring oscillator
*
* filename = [marshall.simox]nist8mod.fil
*
* FILENAME = NMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODN NMOS LEVEL=2 LD=0.250000U TOX=413.000008E-10
+ NSUB=6.294117E+15 VT0=0.807671 KP=4.465000E-05 GAMMA=0.5467
+ PHI=0.6 U0=534.071 UEXP=.16209 UCRIT=90795.9
+ DELTA=1.01989 VMAX=57490.9 XJ=0.250000U LAMBDA=3.494828E-02
+ NFS=5.034625E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=28.380000 CGD0=3.135421E-10 CGS0=3.135421E-10 CGB0=3.907717E-10
+ CJ=9.308500E-05 MJ=0.693518 CJSW=5.398300E-10 MJSW=0.284549 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.28 um
*
* FILENAME = PMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODP PMOS LEVEL=2 LD=0.152257U TOX=413.000008E-10
+ NSUB=7.140277E+15 VT0=-0.807327 KP=2.383000E-05 GAMMA=0.5823
+ PHI=0.6 U0=284.969 UEXP=0.231562 UCRIT=15586.3
+ DELTA=0.920741 VMAX=45761.7 XJ=0.250000U LAMBDA=5.083543E-02
+ NFS=7.553318E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=87.650000 CGD0=1.909559E-10 CGS0=1.909559E-10 CGB0=3.770536E-10
+ CJ=2.500000E-04 MJ=0.545647 CJSW=3.174900E-10 MJSW=0.330136 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.20 um
*
*
* filename = RING.FIL
*
* FILENAME = OUTBUF.FIL
*
.SUBCKT OUTBUF 1 2 3 4 5 6
*
M1 2 1 0 0 MODN L=6.0UM W=6.0UM AD=72P AS=72P PD=36U
+ PS=36U NRD=2.0 NRS=2.0
M2 2 1 3 3 MODP L=6.0UM W=12.0UM AD=144P AS=144P PD=48U
+ PS=48U NRD=1.0 NRS=1.0
R1 2 200 175
C1 200 0 .043P
*
M3 4 200 0 0 MODN L=6.0UM W=12.0UM AD=144P AS=144P PD=48U
+ PS=48U NRD=1.0 NRS=1.0
M4 4 200 3 3 MODP L=6.0UM W=24.0UM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
R2 4 400 250
C2 400 0 .043P
*
M5 5 400 0 0 MODN L=6.0UM W=24.0UM AD=288P AS=288P PD=72U

```

```

+ PS=72U NRD=0.5 NRS=0.5
M6 5 400 3 3 MODP L=6.0UM W=48.0UM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
R3 5 500 350
C3 500 0 .043P
*
M7 600 500 0 0 MODN L=6.0UM W=48.0UM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
M8 600 500 3 3 MODP L=6.0UM W=96.0UM AD=1152P AS=1152P PD=216U
+ PS=216U NRD=0.125 NRS=0.125
R4 600 6 300
C4 6 0 1PF
*
.ENDS OUTBUF
*
* FILENAME = NAND.FIL
*
.SUBCKT NAND 1 2 3 4 5
*
M1 4 1 0 0 MODN L=6.0UM W=24.0UM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
M2 500 1 3 3 MODP L=6.0UM W=48.0UM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
*
M3 500 2 4 0 MODN L=6.0UM W=24.0UM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
M4 500 2 3 3 MODP L=6.0UM W=48.0UM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
R1 500 5 250
C1 5 0 .043P
*
.ENDS NAND
*
* FILENAME = INVERT.FIL
*
.SUBCKT INVERT 1 2 3
*
M1 100 1 0 0 MODN L=6.0UM W=24.0UM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
M2 100 1 3 3 MODP L=6.0UM W=48.0UM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
R1 100 2 250
C1 2 0 .043P
*
.ENDS INVERT
*
*
X25 201 202 3 204 1 NAND
*
X1 1 2 3 INVERT
X2 2 4 3 INVERT

```

```

X3 4 5 3 INVERT
X4 5 6 3 INVERT
X5 6 7 3 INVERT
X6 7 8 3 INVERT
X7 8 9 3 INVERT
X8 9 10 3 INVERT
X9 10 11 3 INVERT
X10 11 12 3 INVERT
X11 12 13 3 INVERT
*
RCIR 13 130 10
CCIR 130 0 .088P
*
X13 130 14 3 INVERT
X14 14 15 3 INVERT
X15 15 16 3 INVERT
X16 16 17 3 INVERT
X17 17 18 3 INVERT
X18 18 19 3 INVERT
X19 19 20 3 INVERT
X20 20 21 3 INVERT
X21 21 22 3 INVERT
X22 22 23 3 INVERT
X23 23 24 3 INVERT
*
X24 24 102 3 104 105 106 OUTBUF
*
RLOOP 24 201 635
CLOOP 201 0 .073P
*
.IC V(1)=5 V(2)=0 V(4)=5 V(5)=0 V(6)=5 V(7)=0 V(8)=5
.IC V(9)=0 V(10)=5 V(11)=0 V(12)=5 V(13)=0 V(14)=5 V(15)=0
.IC V(16)=5 V(17)=0 V(18)=5 V(19)=0 V(20)=5
.IC V(21)=0 V(22)=5 V(23)=0 V(24)=5
*
.IC V(102)=0 V(104)=5 V(105)=0 V(106)=5
*
.IC V(201)=5 V(202)=0 V(204)=0
*
.IC V(3)=5
*
VCC 3 0 5V
VA 202 0 5V
*VA 202 0 PULSE(0V 5V 20NS 5NS 5NS 150NS 200NS)
*
.OPTIONS VNTOL=10UV LIMPTS=500 ITL4=50 ITL5=0
.TRAN 1.0NS 400NS 200NS UIC
*
* node 1   = right after NAND
* node 24  = right before NAND and OUTBUF
* node 106 = OUTPUT

```



```
* node 202 = NAND enabler
*
.PLOT TRAN V(1)
.PLOT TRAN V(24)
.PLOT TRAN V(106)
.PLOT TRAN V(202)
*
.END
```

# APPENDIX J — SPICE File for a Ring Oscillator Using H-Gate MOSFETs

```

*
* Appendix J - SPICE file (named ringhg.cel) for a ring oscillator using H-gate
* MOSFETs
*
* filename = [marshall.simox]nist8mod.fil
*
* FILENAME = NMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODN NMOS LEVEL=2 LD=0.250000U TOX=413.000008E-10
+ NSUB=6.294117E+15 VT0=0.807671 KP=4.465000E-05 GAMMA=0.5467
+ PHI=0.6 U0=534.071 UEXP=.16209 UCRIT=90795.9
+ DELTA=1.01989 VMAX=57490.9 XJ=0.250000U LAMBDA=3.494828E-02
+ NFS=5.034625E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=28.380000 CGD0=3.135421E-10 CGS0=3.135421E-10 CGB0=3.907717E-10
+ CJ=9.308500E-05 MJ=0.693518 CJSW=5.398300E-10 MJSW=0.284549 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.28 um
*
* FILENAME = PMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODP PMOS LEVEL=2 LD=0.152257U TOX=413.000008E-10
+ NSUB=7.140277E+15 VT0=-0.807327 KP=2.383000E-05 GAMMA=0.5823
+ PHI=0.6 U0=284.969 UEXP=0.231562 UCRIT=15586.3
+ DELTA=0.920741 VMAX=45761.7 XJ=0.250000U LAMBDA=5.083543E-02
+ NFS=7.553318E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=87.650000 CGD0=1.909559E-10 CGS0=1.909559E-10 CGB0=3.770536E-10
+ CJ=2.500000E-04 MJ=0.545647 CJSW=3.174900E-10 MJSW=0.330136 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.20 um
*
*
* filename = RINGHG.FIL
*
* FILENAME = OUTBUF.FIL
*
.SUBCKT OUTBUF 1 2 3 4 5 6
*
M1 2 1 0 0 MODN L=6.0UM W=12.0UM AD=144P AS=144P PD=48U
+ PS=48U NRD=1.0 NRS=1.0
M2 2 1 3 3 MODP L=6.0UM W=24.0UM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
R1 2 200 500
C1 200 0 .070P
*
M3 4 200 0 0 MODN L=6.0UM W=12.0UM AD=144P AS=144P PD=48U
+ PS=48U NRD=1.0 NRS=1.0
M4 4 200 3 3 MODP L=6.0UM W=24.0UM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
R2 4 400 575
C2 400 0 .070P
*

```

```

M5 5 400 0 0 MODN L=6.OUM W=24.OUM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
M6 5 400 3 3 MODP L=6.OUM W=48.OUM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
R3 5 500 710
C3 500 0 .070P
*
M7 600 500 0 0 MODN L=6.OUM W=48.OUM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
M8 600 500 3 3 MODP L=6.OUM W=96.OUM AD=1152P AS=1152P PD=216U
+ PS=216U NRD=0.125 NRS=0.125
R4 600 6 300
C4 6 0 1PF
*
.ENDS OUTBUF
*
*
* FILENAME = NAND.FIL
*
.SUBCKT NAND 1 2 3 4 5
*
M1 4 1 0 0 MODN L=6.OUM W=24.OUM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
M2 500 1 3 3 MODP L=6.OUM W=48.OUM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
*
M3 500 2 4 0 MODN L=6.OUM W=24.OUM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
M4 500 2 3 3 MODP L=6.OUM W=48.OUM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
R1 500 5 575
C1 5 0 .070P
*
.ENDS NAND
*
* FILENAME = INVERT.FIL
*
.SUBCKT INVERT 1 2 3
*
M1 100 1 0 0 MODN L=6.OUM W=24.OUM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
M2 100 1 3 3 MODP L=6.OUM W=48.OUM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
R1 100 2 575
C1 2 0 .070P
*
.ENDS INVERT
*
*
*
X25 201 202 3 204 1 NAND
*

```

```

X1 1 2 3 INVERT
X2 2 4 3 INVERT
X3 4 5 3 INVERT
X4 5 6 3 INVERT
X5 6 7 3 INVERT
X6 7 8 3 INVERT
X7 8 9 3 INVERT
X8 9 10 3 INVERT
X9 10 11 3 INVERT
X10 11 12 3 INVERT
X11 12 13 3 INVERT
*
RCIR 13 130 10
CCIR 130 0 .088P
*
X13 130 14 3 INVERT
X14 14 15 3 INVERT
X15 15 16 3 INVERT
X16 16 17 3 INVERT
X17 17 18 3 INVERT
X18 18 19 3 INVERT
X19 19 20 3 INVERT
X20 20 21 3 INVERT
X21 21 22 3 INVERT
X22 22 23 3 INVERT
X23 23 24 3 INVERT
*
X24 24 102 3 104 105 106 OUTBUF
*
RLOOP 24 201 1000
CLOOP 201 0 .073P
*
.IC V(1)=5 V(2)=0 V(4)=5 V(5)=0 V(6)=5 V(7)=0 V(8)=5
.IC V(9)=0 V(10)=5 V(11)=0 V(12)=5 V(13)=0 V(14)=5 V(15)=0
.IC V(16)=5 V(17)=0 V(18)=5 V(19)=0 V(20)=5
.IC V(21)=0 V(22)=5 V(23)=0 V(24)=5
*
.IC V(102)=0 V(104)=5 V(105)=0 V(106)=5
*
.IC V(201)=5 V(202)=0 V(204)=0
*
.IC V(3)=5
*
VCC 3 0 5V
VA 202 0 5V
*VA 202 0 PULSE(0V 5V 20NS 5NS 5NS 150NS 200NS)
*
.OPTIONS VNTOL=10UV LIMPTS=500 ITL4=50 ITL5=0
.TRAN 1.0NS 200NS UIC
*
* node 1 = right after NAND

```



```
* node 24 = right before NAND and OUTBUF
* node 106 = OUTPUT
* node 202 = NAND enabler
*
.PLOT TRAN V(1)
.PLOT TRAN V(24)
.PLOT TRAN V(106)
.PLOT TRAN V(202)
*
.END
```

# APPENDIX K — SPICE File for an SRAM

```

*
* Appendix K - SPICE file (named sram.cel) for an SRAM
*
* filename = [marshall.simox]nist8mod.fil
*
* FILENAME = NMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODN NMOS LEVEL=2 LD=0.250000U TOX=413.000008E-10
+ NSUB=6.294117E+15 VT0=0.807671 KP=4.465000E-05 GAMMA=0.5467
+ PHI=0.6 U0=534.071 UEXP=.16209 UCRIT=90795.9
+ DELTA=1.01989 VMAX=57490.9 XJ=0.250000U LAMBDA=3.494828E-02
+ NFS=5.034625E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=28.380000 CGD0=3.135421E-10 CGS0=3.135421E-10 CGB0=3.907717E-10
+ CJ=9.308500E-05 MJ=0.693518 CJSW=5.398300E-10 MJSW=0.284549 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.28 um
*
* FILENAME = PMODEL.FIL (parameters from NIST8 MOSIS run)
*
.MODEL MODP PMOS LEVEL=2 LD=0.152257U TOX=413.000008E-10
+ NSUB=7.140277E+15 VT0=-0.807327 KP=2.383000E-05 GAMMA=0.5823
+ PHI=0.6 U0=284.969 UEXP=0.231562 UCRIT=15586.3
+ DELTA=0.920741 VMAX=45761.7 XJ=0.250000U LAMBDA=5.083543E-02
+ NFS=7.553318E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=87.650000 CGD0=1.909559E-10 CGS0=1.909559E-10 CGB0=3.770536E-10
+ CJ=2.500000E-04 MJ=0.545647 CJSW=3.174900E-10 MJSW=0.330136 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.20 um
*
*
* filename = sram.fil
*
* FILENAME = OUTBUF.FIL
*
.SUBCKT OUTBUF 1 2 3 4 5 6
*
M1 2 1 0 0 MODN L=6.0UM W=6.0UM AD=72P AS=72P PD=36U
+ PS=36U NRD=2.0 NRS=2.0
M2 2 1 3 3 MODP L=6.0UM W=12.0UM AD=144P AS=144P PD=48U
+ PS=48U NRD=1.0 NRS=1.0
R1 2 200 175
C1 200 0 .043P
*
M3 4 200 0 0 MODN L=6.0UM W=12.0UM AD=144P AS=144P PD=48U
+ PS=48U NRD=1.0 NRS=1.0
M4 4 200 3 3 MODP L=6.0UM W=24.0UM AD=288P AS=288P PD=72U
+ PS=72U NRD=0.5 NRS=0.5
R2 4 400 250
C2 400 0 .043P
*
M5 5 400 0 0 MODN L=6.0UM W=24.0UM AD=288P AS=288P PD=72U

```

```

+ PS=72U NRD=0.5 NRS=0.5
M6 5 400 3 3 MODP L=6.0UM W=48.0UM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
R3 5 500 350
C3 500 0 .043P
*
M7 600 500 0 0 MODN L=6.0UM W=48.0UM AD=576P AS=576P PD=120U
+ PS=120U NRD=0.25 NRS=0.25
M8 600 500 3 3 MODP L=6.0UM W=96.0UM AD=1152P AS=1152P PD=216U
+ PS=216U NRD=0.125 NRS=0.125
R4 600 6 300
C4 6 0 50PF
*
.ENDS OUTBUF
*
*
M1 4 2 1 0 MODN L=6.0UM W=6.0UM AD=72P AS=72P PD=36U
+ PS=36U NRD=2.0 NRS=2.0
M2 4 2 3 3 MODP L=6.0UM W=36.0UM AD=432P AS=432P PD=96U
+ PS=96U NRD=0.33 NRS=0.33
*
M3 2 4 1 0 MODN L=6.0UM W=6.0UM AD=72P AS=72P PD=36U
+ PS=36U NRD=2.0 NRS=2.0
M4 2 4 3 3 MODP L=6.0UM W=36.0UM AD=432P AS=432P PD=96U
+ PS=96U NRD=0.33 NRS=0.33
*
M5 4 5 101 0 MODN L=6.0UM W=6.0UM AD=72P AS=72P PD=36U
+ PS=36U NRD=2.0 NRS=2.0
M6 9 7 101 0 MODN L=6.0UM W=6.0UM AD=72P AS=72P PD=36U
+ PS=36U NRD=2.0 NRS=2.0
*
M7 2 5 201 0 MODN L=6.0UM W=6.0UM AD=72P AS=72P PD=36U
+ PS=36U NRD=2.0 NRS=2.0
M8 10 7 201 0 MODN L=6.0UM W=6.0UM AD=72P AS=72P PD=36U
+ PS=36U NRD=2.0 NRS=2.0
*
X1 101 102 3 104 105 106 OUTBUF
X2 201 202 3 204 205 206 OUTBUF
*
.IC V(1)=0 V(5)=0 V(7)=0 V(9)=0 V(10)=5
.IC V(2)=0 V(4)=5
*.IC V(2)=5 V(4)=0
.IC V(101)=0 V(102)=5 V(104)=0 V(105)=5 V(106)=0
.IC V(201)=5 V(202)=0 V(204)=5 V(205)=0 V(206)=5
.IC V(3)=5
*
VCC 3 0 5V
VLATCH 1 0 PULSE(0V 5V 5NS 5NS 5NS 100NS 200NS)
*VLATCH 1 0 0V
VRWSEL 5 0 PULSE(0V 5V 10NS 5NS 5NS 100NS 200NS)
VWSEL 7 0 PULSE(0V 5V 15NS 5NS 5NS 100NS 200NS)

```

```
*VWSEL 7 0 0V
*
VBIT 9 0 0V
VBITBAR 10 0 5V
*
.OPTIONS VNTOL=10UV LIMPTS=500 ITL4=50 ITL5=0
.TRAN 1.0NS 200NS UIC
*
.PLOT TRAN V(1)
.PLOT TRAN V(2)
.PLOT TRAN V(4)
*
.PLOT TRAN V(101)
.PLOT TRAN V(106)
.PLOT TRAN V(201)
.PLOT TRAN V(206)
*
.END
```







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